Digital Equipment Corporation
Maynard, Massachusetts

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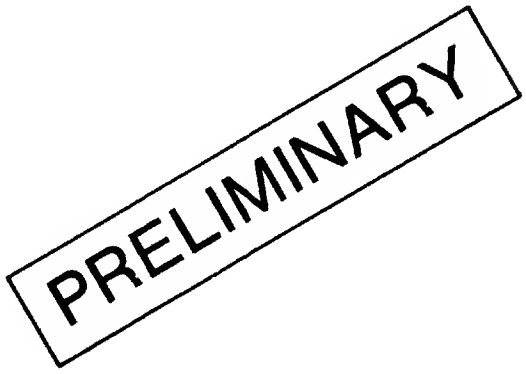
LAB-8/E USER'S HANDBOOK



LAB-8/E
USER'S
HANDBOOK

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FOREWORD

This handbook is intended to familiarize the user with Digital Equipment Corporation (DEC) Laboratory application with the newest and low cost PDP-8/E computer in a laboratory system called LAB-8/E.

CHAPTER 1
SYSTEM INTRODUCTION

Digital Equipment Corporation's LAB-8/E is basically a PDP-8/E with options designed to fulfill the needs of the scientific and engineering communities for a low-cost, modular, easy-to-use laboratory instrument computer. The basic system includes the following:

1. A PDP-8/E General-Purpose 12-bit Digital Computer with a basic 4096 word memory and a 1.2 μs cycle time.
2. A 33 ASR Teletype®, 10 cps Input/Output device with a paper-tape reader and punch.
3. A Laboratory Mounting Panel with precision power supply for use with LAB-8/E peripherals.
4. A 10-bit Analog-to-Digital Converter with sample and hold circuitry and optional multiplexer.
5. A 10-bit Point Plot Display Control for the graphical display of data on an oscilloscope.
6. A Real-Time Clock with five programmable ranges from 1 μs per count to 10 ms per count, plus three Schmitt triggers.

More advanced LAB-8/E systems simply make use of standard PDP-8/E options. Those most commonly used with the LAB-8/E are extra core memory, high-speed paper-tape reader and punch, VR14 large screen display oscilloscope, VR03A modified Tektronix 602 Oscilloscope, and an 8-channel analog multiplexer (expandable to 16 channels).

A chapter of this User's Handbook is devoted to the use of each of the PDP-8/E options used with LAB-8/E. These are the Analog-to-Digital Converter, Point Plot Display Control, Real-Time Clock, and buffered digital I/O. This manual does not cover the use of the PDP-8/E or the rest of the options mentioned. For their use the reader is referred to the PDP-8/E Small Computer Handbook.

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CHAPTER 2
ANALOG-TO-DIGITAL CONVERTER SYSTEM

GENERAL DESCRIPTION

The LAB-8/E Analog-to-Digital Converter allows a user to sample analog data at specified rates and store the equivalent digital value in the PDP-8/E's memory for subsequent processing. Sample and hold circuitry ensures an accurate conversion even on the fastest changing signals by holding the voltage at the input constant until the conversion process is complete.

When used with two eight-channel multiplexer and expander boards, the analog-to-digital converter may select up to 16 analog channels for sampling (refer to Figure 2-1 for illustration showing expanded capability).

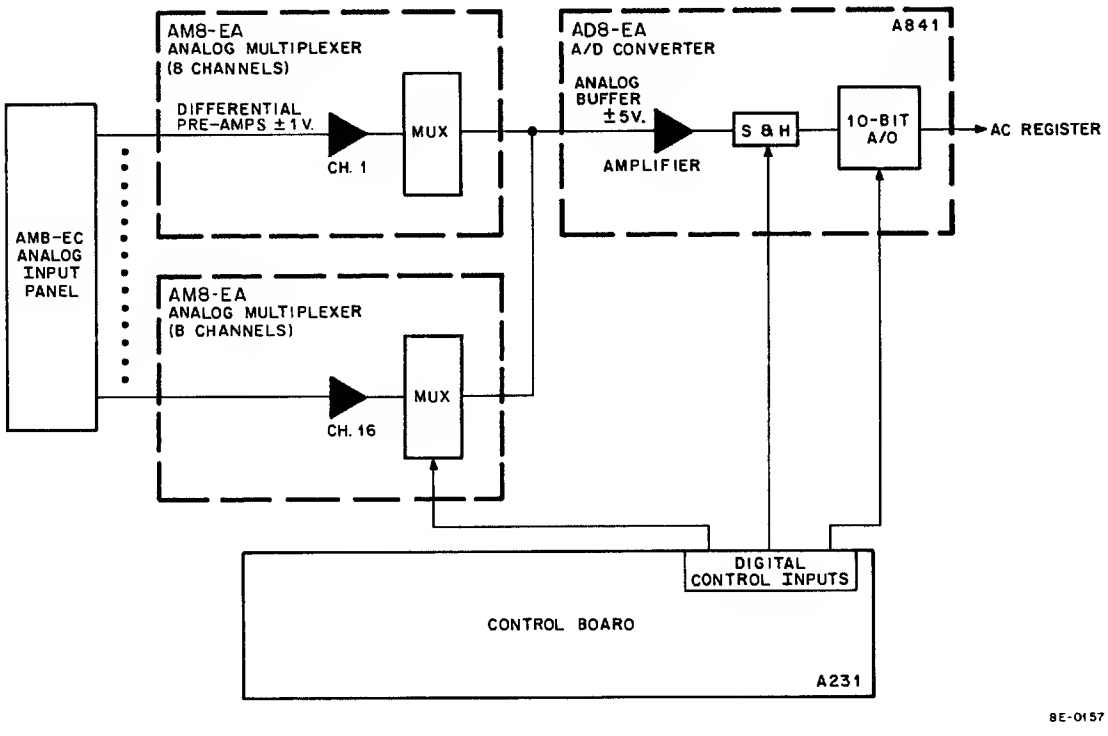


Figure 2-1 A/D Converter and Multiplexer Block Diagram

Input to the LAB-8/E Analog-to-Digital Converter System is via connectors on a panel mounted on the front of the LAB-8/E laboratory mounting panel. When the AD8-EA only is used, the input is differential and in the range

of ±5V. With the AM8-EA multiplexer, the input range is ±1V differential. Also available with the multiplexer are four continuously variable parameter knobs. These knobs control the position of potentiometers which tap a voltage from a standard supply and feed that voltage to the converter system. These knobs are useful to programmers planning to establish parameters, set threshold levels, or move parts of the display. The output of each of these potentiometers is physically connected to a multiplexer channel. Knob 0 connects to channel 0, knob 1 to channel 1, etc. To prevent "hogging" of these multiplexer channels, in the event they are required for external use, a phone jack is associated with each parameter knob. When used externally, the corresponding potentiometer output is disabled and the multiplexer input is available at one common connector input.

AD8-EA ANALOG-TO-DIGITAL CONVERTER

The AD8-EA is a 10-bit successive-approximation converter with sample and hold circuits, conversion circuits, an input buffer and control logic contained on two PDP-8/E modules, A231 and A841. The converter can be used singly with one channel input having an input range of ±5V or can be used with AM8-EA multiplexer boards (A232) to perform conversions for up to 16 channels having full-scale inputs of ±1V. Analog inputs are connected to the module by H851 Edge Connectors from the multiplexer or by a shielded twisted pair from an external device.

Operation of the AD8-EA Converter

Operation of the AD8-EA converter is controlled by IOT instructions. A conversion is initiated by an ADST instruction or from the DK8-ES Real-Time Clock. An input starts the conversion and clears the A/D Done Flag. When the conversion is complete, the converter sets its A/D Done Flag. This flag is sensed by an ADSK instruction. If set, it causes the next instruction to be skipped so that the 10-bit digital word can be transferred to AC2-11 by an ADRB instruction. Since the 10-bit word is in 2's complement form, AC00 and AC01 copy AC02 (sign-extended format). In other words, a negative voltage results in a negative signed number. The converter contains an INTERRUPT ENABLE flip-flop that is controlled by program instructions. When enabled, this flip-flop permits the converter to generate interrupt requests to the program interrupt facility upon completion of a conversion.

The converter also contains circuits for detection of timing errors. A timing error is defined as the receipt of a conversion request or an attempt to change the multiplexer channel while a conversion is in progress. If one of these conditions occurs, the Timing Error Flag is set. The Timing Error Flag is sensed by an ADSE instruction and cleared by an ADCL or ADST instruction.

AD8-EA Specifications

Input Voltage Range	±5V Differential
Input Impedance	Non-Inverting Connection is greater than 10 MΩ in parallel with 300 pF Inverting Input is 10 kΩ in parallel with 300 pF.
Output Format	Parallel: 10 bits right-justified and sign extended, 2's complement.
Resolution	±1/2 LSB at 20°C.
Conversion Rate	Approximately 50 kHz
Sample Acquisition Time	3 μs
Aperture Time	200 ns

AM8-EA 8-CHANNEL ANALOG MULTIPLEXER

The AM8-EA is an 8-channel multiplexer designed to expand the capability of the AD8-EA A/D Converter. The multiplexer accepts bipolar analog inputs having a full-scale range of ±1V and converts these inputs into a full-scale ±5V output supplied to the AD8-EA Converter.

Operation of the AM8-EA 8-Channel Analog Multiplexer

The AM8-EA consists of multiplexer switches and scaling amplifiers for 8 analog channels. The AM8-EA can be expanded up to 16 channels in 8-channel groups by adding an additional AM8-EA 8-channel Multiplexer Expander Module. Multiplexer operation is controlled by the AD8-EA. These instructions and the associated multiplexer control provide the capabilities for random or sequential selection of the multiplexer and reading the active channel address to the computer. Two programmable address modes are provided: auto-increment or non-auto-increment. The AM8-EA is set to non-auto-increment mode when the ADCL command is given.

In the auto-increment mode, channel addresses are incremented automatically at the completion of a conversion by an A/D Done output from the converter. The computer specifies the first channel of interest by issuing an ADLM instruction, then issues A/D converter instructions to start an A/D conversion. Upon completion, the A/D Done Flag increments the multiplexer channel address for the next sample. This process continues until the AUTO MODE flip-flop is reset. Incrementing beyond channel 17_8 causes an automatic reset to channel 0.

AM8-EA Specifications

Input Voltage	Bipolar, ±1V
Input Impedance	Non-Inverting Input is 70 kΩ ±2% in parallel with 300 pF Inverting Input is 35 kΩ ±2% in parallel with 300 pF
Output	Bipolar, ±5V full scale
Common Mode Rejection	Greater than 25 dB, 35 dB (Typical)
Overload Protection	±67V from fault line (Indefinitely)
Overload Recovery Time	8 μs
Frequency Response	Flat from 0 to 30 kHz, -3 dB at 60 kHz
Leakage Current	Negligible at 70Ω impedance
Long Term Stability (one hour)	Not more than 1% for ±30°C change

PROGRAMMING

Eight instructions are used to program the A/D Converter and Multiplexer. Each instruction is completed in 1.2 μs and is defined as follows: (Refer to Figure 2-2 for word format.)

CLEAR ALL (ADCL)

Octal Code: 6530
Operation: Clears the A/D Done Flag and Timing Error Flags to ready the converter for another conversion. This instruction also clears the MUX and Status Register.

LOAD MULTIPLEXER (ADLM)

Octal Code: 6531
Operation: Load Multiplexer Register from AC8-11 and Clear AC.

START CONVERSION (ADST)

Octal Code: 6532
Operation: Clear A/D Done and Timing Error Flags and Start A/D Converter. Channel to be converted is determined by MUX Register.

READ A/D BUFFER (ADRB)

Octal Code: 6533
Operation: Clear A/D Done Flag and load the contents of the A/D Buffer into AC0-11.

SKIP ON A/D DONE (ADSK)

Octal Code: 6534
Operation: Skip the next instruction if A/D Done = 1. Do not clear flag.

SKIP ON TIMING ERROR (ADSE)

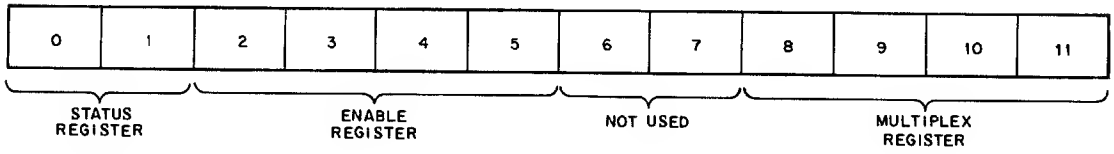
Octal Code: 6535
Operation: Skip the next instruction if Timing Error Flag = 1. Do not clear flag.

LOAD ENABLE REGISTER (ADLE)

Octal Code: 6536
Operation: Load Enable Register from AC2-5 and clear AC Register.

READ STATUS REGISTER (ADRS)

Octal Code: 6537
Operation: Read A/D Status, Enable Register, and MUX into AC0-11.



Status Register
0 – A/D Done Flag Status (Done = 1)
1 – Timing Error Flag Status (Error = 1)

Enable Register
2 – Enable Interrupt on A/D Done = 1
3 – Enable Interrupt on Timing Error = 1 (Note 1)
4 – Enable External (e.g. clock) A/D start
5 – Auto-Increment Mode (Note 2)

Multiplex Register
8–11 – Indicates current channel ($0 - 17_8$) to be sampled by A/D

Figure 2-2 Multiplexer Enable and Status Register Word Format

NOTE 1
The Timing Error Flag indicates that either an ADRB, and ADLM, ADST or external A/D start was attempted while a conversion was in progress. ADLM or ADRB will cause an erroneous result to appear in A/D Buffer while external A/D start or ADST will be ignored.

NOTE 2

When this bit is set, the occurrence of A/D Done = 1 will increment the Multiplex Register by 1. Incrementing past channel 17_8 will cause the MUX register to reset to channel 0.

Programming Examples

Normal Mode – The simplest method of programming the analog-to-digital converter is to have the program issue a start command, loop on the Done Flag until the conversion process is complete and the Done Flag is set to a 1, then the value of the converter's buffer is read into the PDP-8/E accumulator. The program is as follows:

```
ADST        /Clear ADC Done Flag and start conversion
ADSK        /Skip the next instruction when done
JMP-1       /Jump back one instruction
ADRB        /Read ADC buffer into AC
```

If the Analog-to-Digital Converter has been enabled to accept start pulses from an external device, such as a clock, then a timing error could occur. To check for this, the following code could be added after the ADRB command:

```
.
.
.
ADSE        /Skip the next instruction on error
SKP         /Unconditional skip
JMS ERROR   /Go to error routine
.
.
.
```

When the ADC is equipped with the multiplexer option, the channel to be sampled is selected prior to starting the conversion process. This is done using the ADLM command. For example, a simple program to continuously "read" the value of one of the parameter knobs and display the digital value in the PDP-8/E accumulator looks like this:

```
START,  CLA          /Clear the PDP-8/E accumulator
        TAD CHN      /Get the Channel # (0-3 for knobs)
AGAIN,  ADLM         /Load multiplexer from AC
        ADST         /Start
        ADSK         /Skip when finished
        JMP.-1       /
        ADRB         /Read ADC value
        DCA I POINTR /Store this value – POINTR is an Auto-Index
                      Register
        ISZ COUNTER
        JMP AGAIN
```

Clock Mode – In this special mode, an external event, usually the clock overflow, starts the conversion process. The mode samples are taken at regular intervals as defined by the clock rate. The following example takes 1000_{10} samples at the specified clock rate and stores them in memory.

```
                .
                .
                .
INITIALIZE CLOCK AND ADC ENABLE REGISTER
                .
                .
                .
START,          CLA
                TAD NUMBER          /-1000(10)
                DCA COUNTER         /STORE IN COUNTER
                TAD ADDRESS         /ADDRESS OF A/D CONVERSION STORAGE
                                     AREA
                DCA POINTER         /POINTER IS AN AUTO-INDEX REGISTER
ADLOOP,         ADSK                /WAIT FOR CONVERSION DONE
                JMP-1
                ADRB                /READ CONVERSION
                DCA I POINTER       /STORE IT AWAY
                ISZ COUNTER         /HAVE THE REQUIRED # OF SAMPLES
                                     BEEN TAKEN
                JMP ADLOOP          /NO! GET ANOTHER
                .
                .
                .
NUMBER,         -1750(8)            /# OF SAMPLES (1000(10) IN THIS CASE)
COUNTER,        0
ADDRESS,        n-1                 /BEGINNING OF TABLE-1
POINTER,        0
```

CHAPTER 3
DISPLAY SYSTEM

GENERAL DESCRIPTION

The LAB-8/E has a display control called the VC8-E, which is capable of controlling a VR03A or VR14 Display in the form of a 1024_{10} by 1024_{10} dot array. Under program control, a bright spot may be momentarily produced at any point in this array. A series of these intensified dots may be programmed to produce graphical output.

VC8-E POINT PLOT DISPLAY CONTROL

The VC8-E consists of a two-axis, digital-to-analog converter and intensifying circuit (Module M885) that provides deflection and intensity signals. The output of the D/A converters is -5V to +5V in steps of ≈10 mV per step. The signals from the VC8-E are applied to the input amplifier circuitry of such display units as the Type VR03A or the Type VR14 oscilloscopes. The control circuit for the VC8-E is located on a PDP-8/E module (M869). Both modules plug into the OMNIBUS.

The basic system of the VC8-E consists of the following circuitry:

a. OMNIBUS interface, IOT decoding, skip, clear AC, and interrupt control.

b. X-axis buffer, D/A converter, summing amplifier, and bipolar line driver.

c. Y-axis buffer, D/A converter, summing amplifier, and bipolar line driver.

d. Z-axis control, which consists of provision for intensity signal necessary for the VR03A oscilloscope and intensity and channel select signals necessary for the VR14 oscilloscope.

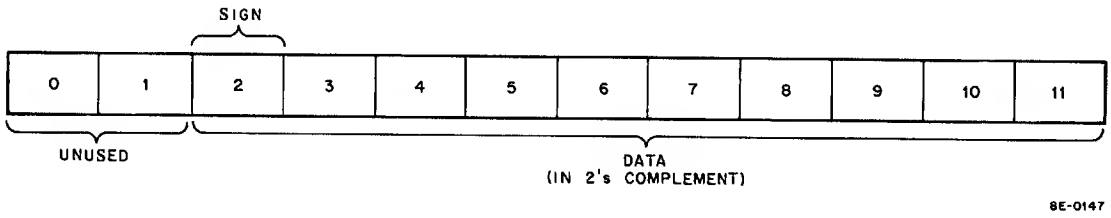
The VC8-E interfaces with the VR03A or the VR14 by means of two different connector assemblies.

The user is reminded of the relationship between the signed octal numbers used above and their corresponding 2's complement form.

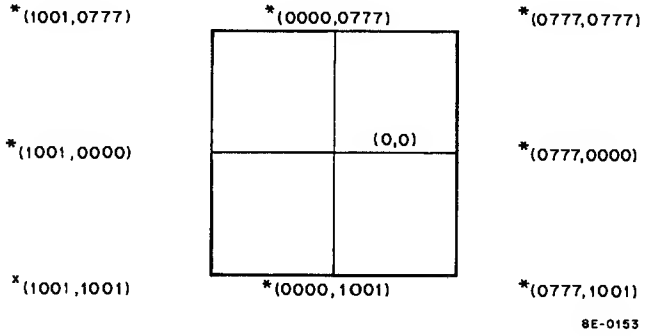
Signed Values (used in example)	2's Complement (10 Bit)	(12 Bit)
+777	0777	0777
.	.	
.	.	
.	.	
+1	0001	1
0	0000	0
-1	1777	7777
.	.	.
.	.	.
.	.	.
-777	1001	7001

OPERATION OF THE DISPLAY SYSTEM

The VC8-E is a two-axis (X and Y), digital-to-analog converter plus intensifying circuitry (Z-axis) that provides deflection and intensity information to the display oscilloscope. Coordinate data (refer to Figure 3-1) is transferred to the X- and Y-axis from bits 2-11 of the PDP-8/E accumulator. This data must be in the range of $\pm 777_8$ and transferred from the rightmost 10 bits of the PDP-8/E accumulator.



The position of the oscilloscope beam will be determined by the contents of the X- and Y-buffer registers. Coordinate (0,0) is located in the center of the screen.



*10 bit 2's complement form

Figure 3-1 Operation of Point Plot Display System

Type VR14 Oscilloscope Display

The VR14 is a compact solid-state CRT display with self-contained power supplies and a viewing area of 6-3/4 in. by 9 in. The VR14 can plot 1500 random points and up to 75 in. of vector with no flicker. Twenty-one μs is required for a maximum deflection step in any direction. Interface with the VC8-E is by means of connector assembly BC01K-10 (10 ft), BC01K-25 (25 ft), or BC01K-50 (50 ft), with 10 ft the standard length.

Type VR03A Oscilloscope Display

The VR03A is a Tektronix Model 602 Oscilloscope Display with mounting hardware for use with the laboratory peripheral panel type H945. The 602 is a solid-state 5 in., 1 MHz display. It provides accurate display of information from X, Y, and Z signal inputs. Interface with the VC8-E is by means of connector assembly BC01L-10 (10 ft), BC01L-25 (25 ft), BC01L-50 (50 ft) or BC01L-A (100 ft), with 10 ft the standard length.

Display Times

The display times of those instructions that include intensification depend on the type of oscilloscope used.

VR14: 21 μs
VR03A: 6 μs

These are the times necessary for the electron gun to reach the specified position before intensification can take place. A switch is provided on the M869 to select the proper interval.

Specifications

Z-Axis (intensity pulse) – The Z-axis polarity is controlled by a switch in the M869 module. The pulse will be either positive or negative depending on the setting. For the VR03A, the switch must be in the positive position; for the VR14, the switch must be in the negative position.

Pulse Width:	1 μs
Pulse Size:	+4V to -2V
Rise Time:	100 ns
Fall Time:	200 ns

NOTE

Provision has been made for controlling a Tektronix Model RM503 Oscilloscope. However, settling time for this unit is somewhat longer than the 21 μs provided for the VR14 settling. A software time delay before intensification must be provided by the user for proper operation. A jumper wire must be removed on the M885 module and another must be installed on two split lugs. This will create a +4V to -10V intensify pulse. With adjustment of the Z-axis intensity on the RM503, the oscilloscope will function.

Digital-to-Analog Converter Specifications

Output Voltage:	+5.01V to -5.01V ±.01V
Resolution:	10 mV ±2.5 mV
Slewing Speed:	<2.5V/μs
Drive Capability:	Capable of driving loads greater than 1 kΩ (min) in parallel with 500[illegible] i.e., 100 ft, 50 pF/ft cable

Offset and gain adjustments provide 10% decrease in range and step sizes and variation of ±.5V from ground.

PROGRAMMING

The instructions for outputting data to the oscilloscope display are defined as follows (refer to Figure 3-2 for Display Enable/Status Register):

Clear All Logic (DILC)

Octal Code: 6050
Operation: Clears enables, flags, and delays

Clear Done Flag (DICD)

Octal Code: 6051
Operation: Clears Done Flag

Skip On Done Flag (DISD)

Octal Code: 6052
Operation: Skip if Done Flag (1). Do not Clear Done Flag.

Load X Register (DILX)

Octal Code: 6053
Operation: Clear Done Flag; load X Register, wait for settle.* Set Done Flag. Do not clear AC.

Load Y Register (DILY)

Octal Code: 6054
Operation: Clear Done Flag; load Y Register, wait for settle.* Set Done. Do not Clear AC.

Intensify (DIXY)

Octal Code: 6055
Operation: Clear Done Flag; intensify; set Done Flag.

Load Enable (DILE)

Octal Code: 6056
Operation: Transfers contents of AC to Enable Register as defined below. Clears AC.

Read Enable/Status Register (DIRE)

Octal Code: 6057
Operation: Transfer the contents of the Display Enable/Status Register to the AC as defined below:

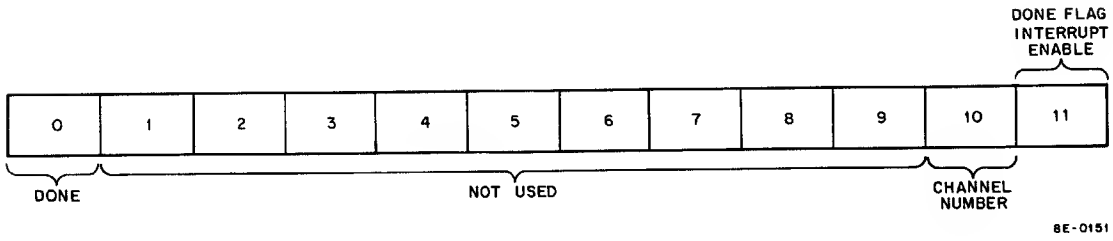


Figure 3-2 Display Enable/Status Register

The Done Flag (bit 0) may be read using a DIRE (transfer enable to AC) command. It may not be set under program control using the DILE (load enable, clear AC) command.

Channel number selects the VR14 display channel. Bit 10 = 0, channel 0; bit 10 = 1, channel 1.

Both channel number and interrupt may be loaded from and read into the AC using the DILE and DIRE commands respectively.

Programming Examples

The VC8-E is a very fast display control. So fast, in fact, that many display oscilloscopes cannot position their beam before an intensify command is performed. For this reason, a Done Flag has been incorporated into the control and should be used whenever random points are plotted sequentially.

The VR03A requires only 8.4 μs to display clear information on the oscilloscope. In applications where the program overhead time is of sufficient length to consume 7 cycles of processor time, there is no need to wait for display Done Flag indications. This is indicated by the following example:

```
        .
        .
        .
CLA
TAD   X                    /GET X-COORDINATE
DILX                       /LOAD X REGISTER
CLA
TAD   Y                    /GET Y-COORDINATE
DILY                       /LOAD Y REGISTER
DIXY                       /INTENSIFY POINT
        .
        .
        .
```

When using the VC8-E with somewhat slower oscilloscopes, such as the VR14, or where there is some doubt concerning the program overhead time, the following code should be inserted prior to an intensify and after the load sequence:

```
        .
        .
        .
DISD                       /SKIP ON DISPLAY DONE FLAG
JMP.-1
        .
        .
        .
```

The following example displays a dot on the screen whose coordinates are set by the position of the ADC's parameter knobs 0 and 1:

```
START,  CLA                /SET AC=0
        JMS   SAMPLE       /POSITION OF KNOB 0
        DILX               /LOAD
        CLA   IAC          /SET AC=1
        JMS   SAMPLE       /POSITION OF KNOB 1
        DILY               /LOAD
        DISD               /SKIP ON DISPLAY DONE FLAG
        JMP -1

        DIXY               /INTENSIFY
        JMP   START

SAMPLE, 0
        ADLM               /LOAD MULTIPLEXER
        ADST               /START CONVERSION
        ADSK               /WAIT
        JMP. -1
        ADRB               /READ
        JMP I              SAMPLE
```

Kaleidoscope is an amusing program for the VC8-E. Pictures on the screen are varied by manipulating the switch register bits 9, 10, and 11.

```
/KALEIDOSCOPE PROGRAM

START,  TAD     Y       /GET Y
        JMS     SCALE   /SCALE IT
        CMA             /2's COMPLEMENT
        TAD X           /CONFUSE WITH X
        DCA X
        TAD X
        DILX            /LOAD X
        JMS     SCALE   /SCALE
        TAD Y           /CONFUSE WITH Y
        DILY            /LOAD Y
        DISD
        JMP. -1
        DIXY            /INTENSIFY
        DCA Y
        JMP     START   /DO AGAIN

SCALE,  0
        DCA     TEM     /TEMP STORE
        OSR             /READ SWITCHES
        CIA             /NEGATE
        DCA     C       /STORE
        TAD     TEM     /GET VALUE TO CHANGE
CHANGE, CLL
        SPA
        CML
        RAR
        ISZ     C
        JMP     CHANGE
        JMP I   SCALE

        X,2222
        Y,1111
```

CHAPTER 4
REAL-TIME CLOCK

GENERAL DESCRIPTION

The LAB-8/E Real-Time Clock option offers the PDP-8/E user a method for accurately measuring and counting intervals or events in a number of ways. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events or provide program interrupts at programmable intervals. Some of these operations can be performed concurrently.

OPERATION OF REAL-TIME CLOCK

Logically, the DK8-ES contains the following features:

Clock Counter Register

The Clock Counter Register (refer to Figure 4-1) is one of the four registers in the DK8-ES that are accessible to the program. Each generated pulse causes the clock counter to be incremented by 1. The counter increments up to 7777_8 and then "overflows" on the next pulse, causing the "overflow flip-flop" or flag to be set to 1. The Overflow Flag being set is program detectable and can be sensed by a program interrupt, a skip instruction and/or a read status instruction. The contents of the clock counter at any given point may be determined by an instruction that puts the contents of the clock counter into the AC via the Buffer-Preset Register. The contents of the Clock Counter Register may also be set by the user via the Buffer-Preset Register and the Clock Control Register.

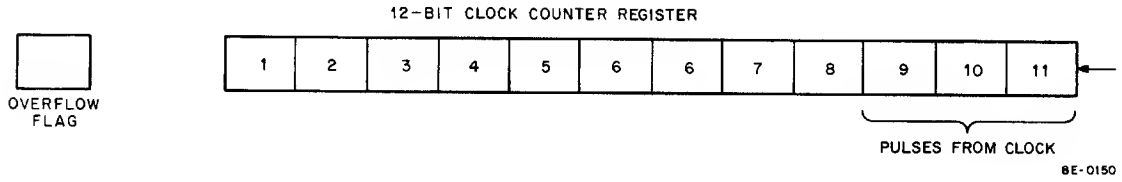


Figure 4-1 12-Bit Clock Counter Register

Buffer-Preset Register

The 12-Bit Buffer-Preset Register is the link between the processor, accumulator, AC, and the clock counter (refer to Figure 4-2). It is used to read the contents of the Clock Counter Register into the AC. It is also used to buffer the current count in the clock counter when this value is to be saved. It is then made available to the program by an instruction that reads the Buffer-Preset Register into the AC. Another use is made of this register in holding the number to be transferred into the clock counter each time the counter overflows. This number is loaded into

the Buffer-Preset Register from the AC. This allows the counter to be reset to some desired starting value each time the counter overflows. This gives the program a highly flexible control over the apparent clock frequency.

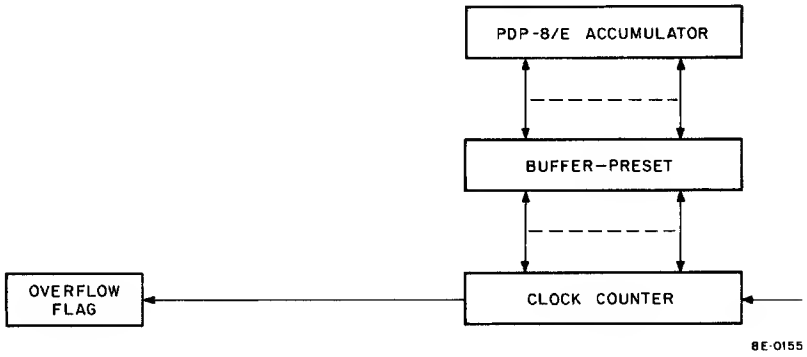


Figure 4-2 Operation of Buffer-Preset Register

Clock Enable Register

The Clock Enable Register (refer to Figure 4-3) is the 12-bit register that determines the "who, what, when and how" of the clock.

This register controls the rate of the time base and the mode of counting, and selectively enables each of the three input channels and the interrupt line. Other bits in the 12-bit register determine interrupt and enable conditions. The Clock Enable Register is loaded from the PDP-8/E accumulator under program control. The conditions enabled for any channel determine what action must be taken to detect an event.

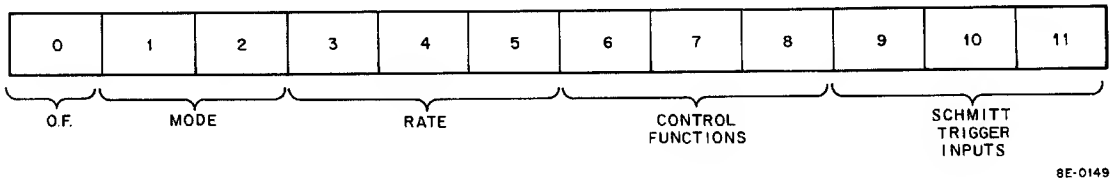


Figure 4-3 Clock Enable Register Word Format

Mode Selection – Bits 1 and 2 of the Enable Register can be considered the "Mode Control Register", which is used to determine the method by which the clock operates.

AC Bit	Function
0	Enables clock overflow to set corresponding bit in the Status Register.
00	Free Run – the counter is incremented at the specified rate.
	Counting goes from 0 to 7777_8 and then overflows and starts counting from 0 again. Overflow, therefore, occurs every 4096_{10} counts (or every 4096 x counting rate cycles).

AC Bit	Function
00 (cont)	The overflow flag remains set until cleared by programming.

0000 ⟶ 7777 ⟶ OVERFLOW

01 Present Time – as in mode 00, the counter is incremented at the specified rate.

Each time overflow occurs, however, the contents of the Buffer/Preset Register are transferred automatically to the counter, which then continues counting up from that value. The Buffer/Preset Register is usually set to the negative (2's complement) value of the number of counts desired before overflow. In this mode, the user has not only determined the rate of counting but also the number of counts before overflow, thus allowing him two dimensions in selecting the time intervals between overflow (refer to Figure 4-4).

In this mode, as in mode 00, the overflow remains set until cleared by programmer.

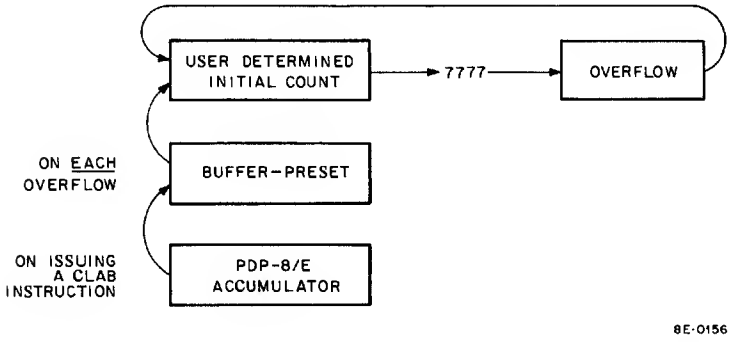
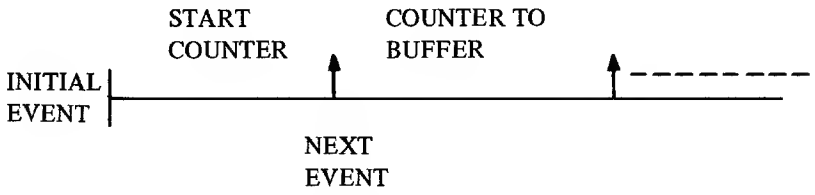


Figure 4-4 Partial Diagram Showing Major Components of Real-Time Clock

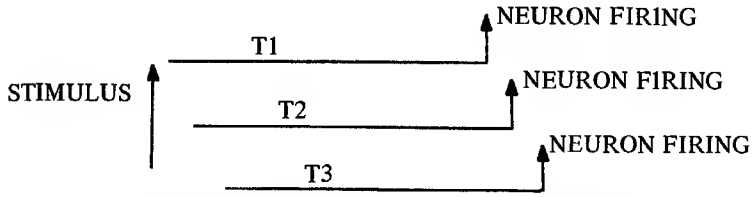
10 Time Base from initial event – as in modes 00 and 01, the clock counter is incremented at the specified rate, but on each occurrence of an input event on a selected input channel (Schmitt trigger) the contents of the clock counter are automatically transferred to the Buffer/Preset Register and the counter continues to count.



This mode is useful for determining the total elapsed time between some initial event (a stimulus possibly) and subsequent events that might be caused by it (muscle reactions). In using mode 10, the Clock Status Register is used in conjunction with the Clock Enable Register to detect the occurrence of the input events. Each time such an event is recognized, the contents of the Buffer/Preset Register can be picked up by the program and stored away or processed as the user wishes.

AC Bit	Function

A poststimulus histogram (PST) could be generated in this fashion. A stimulus could be issued to a subject, and the clock started. Then the elapsed time to succeeding neuron firings (i.e., input events) could be determined by saving the time counts that were transferred from the counter to the Buffer/Preset on each firing.



11 Time Base between two events – as in modes 00, 01, and 10 the clock counter is incremented at the specified rate.

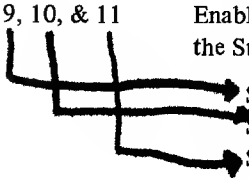
On each occurrence of an input event on a selected input channel (Schmitt trigger), the contents of the clock counter are automatically transferred to the Buffer-Preset Register. This is identical to mode 10 so far.

Here is where mode 10 and mode 11 differ. In mode 10, the clock counter continues to count after the transfer, no matter on which of the three enabled input channels the event occurred. In mode 11, the clock counter is cleared after being transferred to the Buffer-Preset Register; counting then continues from 0 at the specified rate (refer to Table 4-1 for rate selection).

Table 4-1
Rate Selection

Contents of Bits 3-5	Octal Value	Interval Between Pulses	Frequency
000	0	Stop	0
001	1	---	External Input
010	2	10^{-2} sec	100 Hz
011	3	10^{-3} sec	1 kHz
100	4	10^{-4} sec	10 kHz
101	5	10^{-5} sec	100 kHz
110	6	10^{-6} sec	1 MHz
111	7	Stop	0

AC Bit	Function
6	Enable external start, (of AD8-E).
7	Inhibits the clock from counting when set to a 1. Bit 7 is cleared by firing any enabled Schmitt trigger.
8	Causes an interrupt request when any bits in the Status Register are set to a 1.
9, 10, & 11	Enable the firing of Schmitt triggers 1, 2, or 4 to set corresponding bits in the Status Register.



NOTE

The program interrupt facility must have been enabled by issuing an ION (6001) before an actual program interrupt can occur. If an ION has been issued, Enabling Interrupt on an input Channel or on Overflow will still cause the Clock Flag to be set to I, but the program will JUMP to a subroutine at 0. The Clock Flag can be checked, like any other device flag, with a skip on flag = I instruction CLSK.

Any or all of the Schmitt triggers may be enabled to set the Clock Status Regsiters. Depending on other bits set in the ENABLE register, this may cause an interrupt or a transfer of clock counter information to the Buffer-Preset Register.

Schmitt Triggers

We have done a lot of talking about Schmitt trigger input channels without explaining too much about the Input Channels themselves or about what determines an event. Let us now turn to the Input Control Panel which is mounted on the Laboratory Mounting Panel. It is labeled "Schmitt triggers" in white printing and has three groups of white outlined boxes delineated on it, each with a similar set of controls. Each represents one input channel to which an external signal may be connected. Within each box there is a phone jack (Differential Input) marked "input" and a BNC marked "output", a switch marked "slope" and a control knob marked "threshold". The input jacks have the following specifications:

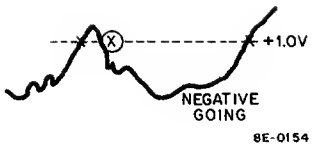
Input Threshold	Variable between ±5V
Source	+, -,
Input Type	Differential
Input Resistance	50K
Minimum Duration Input Pulse	2 μs
Maximum Permissible Input Voltage	±50V
Hysteresis	0.3V
Common Mode Rejection	35 dB
Propagation	600 ns
Output Voltage	0 to +5V (falling edge denotes firing and resets on recrossing the threshold voltage).

NOTE

There is no need to enable a Schmitt trigger to make use of its signal conditioning properties. An analog signal may be used to drive the external clock input by connecting to the analog signal to the Schmitt trigger input, and then connecting the output to the external clock input.

The Schmitt trigger "firing" (refer to Figure 4-5) is governed by the setting of the "source" and "threshold" controls. A voltage between +5V and -5V is coarsely selected by setting the threshold knob to the far right for +5V, far left for -5V, or at some point in between. The slope, either positive-going or negative-going, is then chosen by setting the slope switch to either + or -. At this point, each time the external signal crosses the preset voltage in the indicated direction, the Schmitt trigger will fire, causing a pulse to be generated. This is the pulse which we have been speaking of as an event.

Other Enable bit functions are covered under the next section on Clock Programming.



*If threshold was set to +1 V and slope to +, then the *'s indicate a pulse generated while the Ⓧ does not. Even though the threshold was crossed, the second condition of slope was not satisfied and so a pulse was not produced.

Figure 4-5 Schmitt Trigger Definition

Clock Status Register

The Clock Status Register (see Figure 4-6) is essentially the "who done it" register of the clock.

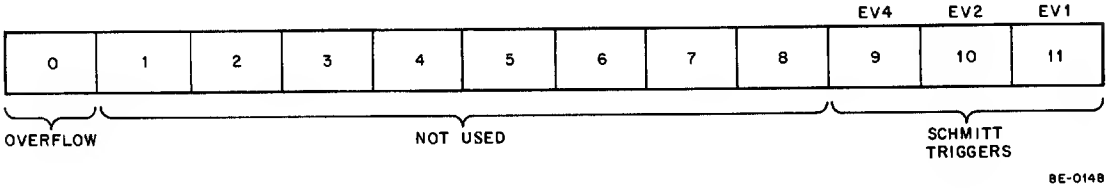


Figure 4-6 Clock Status Register

PROGRAMMING

The following IOT instructions control the DK8-ES Real-Time Clock:

Clear Clock Enable Register per AC (CLZE)

Octal Code: 6130
Operation: Clears the bits in the Clock Enable Register corresponding to those bits set in the AC. The AC is not changed.

Skip on Clock Interrupt (CLSK)

Octal Code: 6131
Operation: Causes the next instruction to be skipped if an interrupt condition exists.

a. An enabled Schmitt trigger has fired.
b. The clock counter has overflowed.

Set Clock Enable Register per AC (CLOE)

Octal Code: 6132
Operation: Sets the bits in the Clock Enable Register corresponding to those bits set in the AC. The AC is not changed.

AC to Clock Buffer-Preset (CLAB)

Octal Code: 6133
Operation: Causes the contents of the AC to be transferred into the Clock Buffer-Preset; then causes the content of the Clock Buffer-Preset to be transferred into the clock counter. The AC is not changed.

Load Clock Enable Register (CLEN)

Octal Code: 6134
Operation: Causes the content of the Clock Enable Register to be transferred into the AC.

Clock Status to AC (CLSA)

Octal Code: 6135
Operation: Interrogates the Clock Input and Overflow Status flip-flops. The Clock Status information is inclusively ORed into the AC, then all status bits are cleared. This ensures that only one occurrence of an event will be transferred to the program. The status condition is established as follows:

AC Bit	Status Condition
0	Overflow
9	Event 4
10	Event 2
11	Event 1

Clock Buffer to AC (CLBA)

Octal Code: 6136
Operation: Clears the AC, then transfers the content of the Clock Buffer into the AC.

Clock Counter to AC (CLCA)

Octal Code: 6137
Operation: Clears the AC, transfers the content of the Clock Counter to the Clock Buffer, then transfers the content of the Clock Buffer into the AC.

NOTE

The clock counter may be read while it is counting. Gating in the clock control section prevents data from being strobed out of the counter before a specified time following a clock pulse. This time, approximately 300 ns, allows the data to be settled in the counter.

This feature allows the counter to be read any number of times without introducing timing errors in counting; the amount of time between intervals, and also eliminates false counts that are the result of reading the counter as one or more bits are in transition from one state to another.

Programming Examples

Example Subroutine #1 – This example illustrates how the DK8-ES can be used as a double-precision (24-bit) free-running clock, using the clock counter as the low order 12 bits and a memory location as the high order 12 bits. Because all of the clock's registers have been set to 0 initially by the clear key, the program needs only to 0 the high order words, set the enable register, and turn on the interrupt. After 4096 counts, the clock counter overflows, signalling an interrupt. The service routine simply increments the high order word, then returns to the main program.

```
            * 1
            JMP I 2
            SERVC                   /POINTER TO INTERRUPT SERVICE ROUTINE

            *200
START,      CLA CLL
            DCA HIGH                /ZERO HIGH ORDER WORD
            TAD ENABLE
            CLOE                    /LOAD ENABLE REGISTER
            CMA                     /CLEAR UNUSED BIT
            CLZE
            ION                     /AND TURN ON INTERRUPT
          MAIN PROGRAM
                .
                .
                .
                .
SERVC,      CLSK                    /WAS INTERRUPT CAUSED BY CLOCK FLAG?
            JMP RETURN              /NO
            CLSA                    /READ STATUS, IGNORE FLAG AND CLEAR IT
            SPA CLA                 /WAS STATUS REGISTER NEGATIVE?
            ISZ HIGH                /YES, INCREMENT THE HIGH ORDER WORD
            JMP RETURN              /AND RETURN IF HIGH DID NOT OVERFLOW
            JMP SOMEWHERE           /AFTER 4096*4096 COUNTS, DO SOMETHING
RETURN,     ION
            JMP I 0
ENABLE,     4110                    /OVERFLOW, + MODE 00 + 100 Hz RATE +
                                     INTERRUPT ENABLE
HIGH,       0
```

With this simple program, time can be kept during program execution. With the clock set to its fastest rate (1 μs per tick), this double-precision counter could mark time for only just over 16 seconds; with the clock set to its slowest rate, it could mark time for over 100 days.

A simple routine could be written to interrogate elapsed time by using the CLCA (Clock Counter to AC) command.

Example Subroutine #2 – The DK8-ES can also easily be programmed to function as an alarm clock, counting off a period of time, giving an alarm, automatically resetting itself, and continuing. The alarm could be used to ring a bell, as indicated in the example; however, a more practical use would be to start an analog-to-digital converter to take a number of samples from the outside world.

This example will ring the bell every second:

```
START,      CLA
            TAD COUNTER             /SET COUNTER TO -1000
            CLAB
            CLA
            TAD ENABLE              /SET ENABLE REGISTER
            CLOE
AGAIN,      CLSK                    /CLOCK SKIP?
            JMP. -1
            CLSA                    /YES, READ STATUS AND CLEAR IT
            CLA
            TAD BELL                /RING BELL
```

(continued on next page)

```
                TLS
                TSF
                JMP. -1
                JMP AGAIN
COUNTER,        -1750
ENABLE,         OVERFLOW + MODE 01 + 1 ms = 5600
BELL,           207
```

This program could easily be modified to work in the interrupt mode by setting bit 8 of the Enable Register to a 1. An interrupt would then occur every second and a service routine could be used to ring the bell.

CHAPTER 5
12-CHANNEL BUFFERED DIGITAL I/O

GENERAL DESCRIPTION

The DR8-EA Digital I/O can be used to control 12 discrete digital switching circuits located externally and can be used to accept 12 discrete digital inputs from external sources. The unit consists of IOT control logic, a 12-bit input buffer, a 12-bit output buffer, and 3 multiplexer ICs that control the flow of data for input and output operations. All circuits are TTL logic and are mounted on a single PDP-8/E module, which plugs into the OMNIBUS. The standard TTL outputs are connected to the external load via two H854 connectors on the module. Inputs from external sources are also connected to the DR8-EA, using H854 connectors.

A maximum of 8 DR8-EA options can be used. Each device selector code is determined by the user by means of jumpers. Device codes 50 to 57 are legal; however, the DR8-EA normally comes with device code 50 installed.

The DR8-EA is contained entirely on one 8-1/2 in. Quad type board (M863). The module may be used in the PDP-8/E OMNIBUS, BE8 expanded OMNIBUS, or BA8 expander.

OPERATION OF DR8-EA

Refer to Figure 5-1 for block diagram.

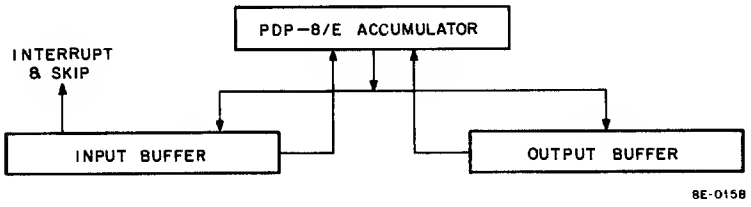


Figure 5-1 12-Channel Buffered Digital I/O

Output Transfers

Data outputs are updated under program control. Standard output drivers have a TTL 30-unit load capability. For an output function the computer issues a DBR0, DBS0, or DBC0 instruction. For DBS0 instructions, only logical 1s in the AC are loaded into the output register; AC bits containing logical 0s do not affect output register bits. For DBC0 instructions, logical 1s in the AC result in logical 0s in corresponding bits of the output register. For DBR0 instructions, the contents of the output register is transferred into the AC register.

Input Transfers

Data inputs must be TTL compatible, have negative transition to .8V or less for a logical 1, and have a pulse duration of greater than 50 ns. Pulse rise and fall time should be less than 150 ns for maximum noise immunity. In one mode of operation, the input register bits, once set by the data inputs, remain set until read by a DBRI instruction and cleared by a DBCI instruction. In the second mode of operation, the input can be placed directly through gating on the bus and will remain as long as the input remains. The DBRI instruction is also used to read the input data. When this IOT is issued, the contents of the input register are gated to the AC via the OMNIBUS. A DBCI instruction, used with DBRI instruction, enables inputs that occurred too late to be read by the next DBRI instruction, providing that the frequency of input data is greater than the time elapsed between the issuing of the DBRI and DBCI. Correct usage of this feature results in "zero dead time" for events. Any of the input lines can cause an interrupt if the proper jumpers are selected. The interrupt facility can be enabled by instruction DBEI and disabled by instruction DBDI.

SPECIFICATIONS

Input Format:	Parallel, 12 bits
Input Levels:	Compatible TTL levels. Input lines clamped at -0.6V to +5V for negative input protection.
Input Connections and Pulse Width:	Inputs to inverter buffers are normally held high by resistors. A negative transition of 0.8V or less will cause the input to become a logical 1. Optional inputs bypass the flip-flop for direct interrogation of input line status.
Output Format:	Parallel, 12 bits
Output Levels:	TTL-compatible levels capable of driving 30 unit loads. Output lines are protected from short circuits to ground.
Environmental:	0°C to 55°C 10% to 90% relative humidity (non-condensing)
Power Requirements:	+5.0V, 2.25A (Worst case)

Jumper Descriptions

The chart defined below will enable the user to change the IOT device code by changing the jumper across the specified split lug.

Device Selector		Jumper		
(normal conf)	50	6H	7H	8H
	51	6H	7H	8L
	52	6H	7L	8H
	53	6H	7L	8L
	54	6L	7H	8H
	55	6L	7H	8L
	56	6L	7L	8H
	57	6L	7L	8L

The normal configuration will be factory installed with device selector code 50.

The input jumpers will be factory installed with A jumper, (edge triggered flip-flop). To change to level enables, use jumper B. The A, B, lugs are on all 12 bits.

Jumpers will also be provided to insulate the inputs from the interrupt and skip circuitry.

PROGRAMMING

The following instructions are used for DR8-EA operation. The X refers to a jumper selectable code. However, the DR8-EA normally comes with code 50 installed.

Disable Interrupt (DBDI)

Octal Code: 65X0
Operation: Disable all interrupts that are caused by a logical 1 on the input.

Enable Interrupts (DBEI)

Octal Code: 65X1
Operation: Set Interrupt Enable Flip-Flop. This tests the IN FLAG and causes an Interrupt Request if IN FLAG equals 1.

Skip on Flag (DBSK)

Octal Code: 65X2
Operation: Tests the IN FLAG. If the Flag is a 1, the next sequential memory location is skipped.

Clear Selective Input Register (DBCI)

Octal Code: 65X3
Operation: 1s in the AC clear respective bits in the Input Register.

Transfer Input to the AC (DBRI)

Octal Code: 65X4
Operation: Transfers the complete 12-bit Input Register to the AC.

Clear Selective Output Register (DBCO)

Octal Code: 65X5
Operation: 1s in the AC clear the respective bits in the Output Register.

Set Selective Output Register (DBSO)

Octal Code: 65X6
Operation: 1s in the AC set the respective bits in the Output Register.

Transfer Output to AC (DBRO)

Octal Code: 65X7
Operation: Transfer the complete 12-bit Output Register to the AC.

Programming Examples

Example 1: Assume that 10 bits of digital information is to be transferred to the PDP-8/E. When the data is ready, the occurrence of one of two possible pulses defines this information.

Solution: Define *input* bits 2–11 as data and remove the interrupt jumpers. Define *input* bit 0 as process one and this will cause an interrupt. Define *input* bit 1 as process two and this will also cause an interrupt. Define *output* 0 as the data accepted pulse.

```
SET UP,     CLA CLL          /CLEAR THE AC AND THE LINK
            CMA              /ALL ONES THE AC
            DBCI             /CLEAR THE INPUT REGISTER
            DBCO             /CLEAR THE OUTPUT REGISTER
            DBEI             /ENABLE THE INTERRUPTS IN DR8-EA
            ION              /TURN ON INTERRUPTS
            JMP Program      /JUMP TO PROGRAM THAT WAITS FOR DATA
```

When an interrupt occurs the program goes to the location specified and jumps to the interrupt handling routine.

```
            DBSK             /SKIP ON AN INPUT FLAG
            SKP              /SKIP
            JMP INPUT        /GO TO DATA PROCESSING ROUTINE
```

Data processing routine will define and accept the data.

```
INPUT,      CLA,CLL          /CLEAR THE AC AND LINK
            DBRI             /TRANSFER TO AC
            DBCI             /CLEAR THE BITS THAT WERE SET
            DCA TEMP         /STORE
            DBDI             /DISABLE INTERRUPT
            TAD4000          /BIT 0=1
            DBSO             /CREATE START OF PULSE
            DBCO             /END THE PULSE
                             (1.2 μs pulse)
            CLA, CLL         /CLEAR AC & LINK
            TAD TEMP         /ADD IT TO THE AC
            SMA              /CHECK FOR BIT 0 = 1
            JMP P2           /JUMP TO PROCESS TWO
            JMP P1           /JUMP TO PROCESS ONE

            The data is then in process

P2,         CLA
            TAD TEMP         /ADD TOTAL REGISTER
            AND K1777        /MASK FOR DATA
            DCA DATA         /STORE IT
```

Example 2: Twelve random events may occur at any time; we wish to control their corresponding output functions.

Solution: Define the same corresponding input and output bits; i.e., bit 0 input event – bit 0 output function.

```
SET UP,     CLA,CLL          /CLEAR THE AC AND THE LINK
            CMA              /ALL ONES IN THE AC
            DBCI             /CLEAR THE INPUT REGISTER
            DBCO             /CLEAR THE OUTPUT REGISTER
            DBSK             /SKIP ON A FLAG
            JMP .-1          /GO BACK

INPUT,      CLA, CLL         /CLEARS THE AC AND LINK
            DBRI             /GET THE INFORMATION (to AC)
            DBSO             /SET CORRESPONDING OUTPUT BIT
            DBCO             /CLEAR CORRESPONDING OUTPUT BIT

            (We just created an output pulse)
```

(continued on next page)

```
DBCI                    /CLEAR INPUT BIT
JMP Program             /ENABLES THE INTERRUPT

.
.
.
CONTINUE (DETECT OTHER EVENT)
```

INTERFACE

The DR8-EA interfaces to the PDP-8/E OMNIBUS by plugging directly into the bus.

Interface to the outside word is provided by two edge connectors on the M863 module. Signals leaving the board (12 bits parallel) are high (+3V) for a logical false and ground (0V) for a logical true. Each output line has approximately 20 mA of drive (high level) and 20 mA of sink (low level). Output levels remain fixed except when changed by the processor.

Signals entering from the outside world must be in TTL format. The input represents approximately two unit loads. When jumpered for "edge detection", a negative-going edge (3V to 0V) is sensed. The signal must remain low (0V) for at least 50 ns. When sensing for an external level (jumpered to bypass the flip-flop), ground (0V) represents a logical true and a high (+3V) represents a logical false. With all bits jumpered in this manner, the option represents a 12-bit parallel input register rather than an event detector.

Two optional means of interfacing to the DR8-EA are available. The first option is two BC08J-X cables. Each cable (ribbon-type) is terminated by a Berg-type connector on one end (for interfacing to the DR8-EA module) and a standard DEC Flip-Chip on the other. One cable is used for the input and the other for output.

Cable Descriptions

The 7008418 cable will be used to jumper to input to the output for diagnostic purposes. It will be part of the DR8-EA option. If the user desires interface cables the following can be purchased.

The BC08J cable consists of the 1210073-0 Berg connector, cable and the M953 module.

PIN CONNECTIONS

J2 – Input	J1 – Output
D – Bit 0	D – Bit 0
F – Bit 1	F – Bit 1
J – Bit 2	J – Bit 2
L – Bit 3	L – Bit 3
N – Bit 4	N – Bit 4
R – Bit 5	R – Bit 5
T – Bit 6	T – Bit 6
V – Bit 7	V – Bit 7
X – Bit 8	X – Bit 8
Z – Bit 9	Z – Bit 9
BB – Bit 10	BB – Bit 10
DD – Bit 11	DD – Bit 11

The output and input pins corresponding to the AC bits enabled on the M863 (DR8-EA) are as follows:

Input and Output End Pins (BC08J)

Bit 0 – B1
Bit 1 – D2
Bit 2 – D1
Bit 3 – E2
Bit 4 – E1
Bit 5 – H2
Bit 6 – H1
Bit 7 – K2
Bit 8 – J1
Bit 9 – M2
Bit 10 – L1
Bit 11 – P2

Gnds A1, C1, F1, K1,
N1, R1, T1, C2,
F2, J2, L2, N2,
R2, U2

CHAPTER 6
LABORATORY MOUNTING PANEL

The laboratory peripheral panel is designed for compact yet versatile packaging of modular accessory equipment for laboratory environments. The panel is a 19-in. rack-mounted unit with H945 panel mounting frame and housing that accepts plug-in type modules or module panels. Modules can be single-width, double-width, or other multiples of single-width, and may contain a printed circuit card mounted on the vertical dimension. Controls and input/output connectors for peripheral equipment are mounted on the module front panel. Modules or module panels are attached to the panel frame using one fastener at the top and bottom of the module panel.

The following options are available:

H945	Housing (rack-mountable chassis) for mounting laboratory peripherals including space for mounting 11 panel units; 5 single-panel units; 3 double-panel units, and a single 1-1/2 panel unit filler panels.
H945-BA	115V Table-Top version with super cover.
H945-BB	230V Table-Top version with super cover.
H945-CA	115V Rack-Mounted version.
H945-CB	230V Rack-Mounted version.
AM8-EC	Analog input panel – 16-channel A/D panel used for AM8-EA multiplexer inputs. Panel contains four 3-conductor phone jacks and four 10-turn vernier controls and 2 connectors. Panel requires 3 single-panel unit widths.
AM8-ED	Simple Analog Input Panel 16-channel A/D panel used for AM8-EA multiplexer inputs. Panel contains two connectors and requires a single-panel unit width.
VR03-A	Model 602 Tektronix Oscilloscope and VM03 Mounting Hardware.
VM03	Model 602 Tektronix Oscilloscope Mounting Hardware.
VR14	115 Vac CRT Display with mounting hardware for Rack-Mounted version.
VR14-A	230 Vac CRT Display with mounting hardware for Rack-Mounted version.
VR14-B	100 Vac CRT Display with mounting hardware for Rack-Mounted version.
VR14-C	115 Vac CRT Display with mounting hardware for Table-Top version.
VR14-D	230 Vac CRT Display with mounting hardware for Table-Top version.
VR14-E	100 Vac CRT Display with mounting hardware for Table-Top version.

MAY 1, 1971

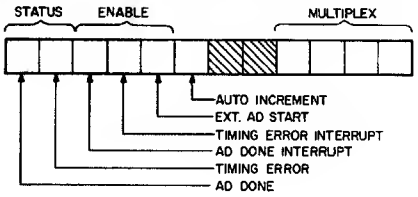
lab8/e

INSTRUCTION LIST

ANALOG TO DIGITAL CONVERTER (AD8-EA/AM8-EA)

ADCL	6530	Clear all
ADLM	6531	Load multiplexer from AC, clear AC
ADST	6532	Start AD conversion, Clear Done
ADRB	6533	Read AD Buffer
ADSK	6534	Skip on AD done
ADSE	6535	Skip on timing error
ADLE	6536	Load AD-enable register, Clear AC
ADRS	6537	Read enable, status and MUX

MULTIPLEX, ENABLE AND STATUS REGISTER



Status register:
- 0—set if AD is done
- 1—timing error flag

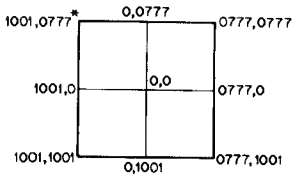
Enable register:
- 2—enable interrupt on AD done
- 3—enable interrupt on timing error
- 4—enable ext. AD start (clock)
- 5—auto-increment multiplexer

Multiplex register:
- bits 8-11

indicates current AD channel to be sampled ($0\text{-}17_8$)

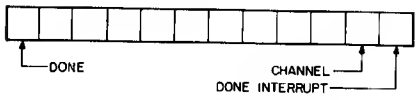
DISPLAY CONTROL (VC8E)

DICL	6050	Clears enables, flags
DICD	6051	Clears done flag
DISD	6052	Skip on display done flag (no clr)
DILX	6053	Load x register
DILY	6054	Load y register
DIXY	6055	Intensify
DILE	6056	Load enable from AC, clear AC
DIRE	6057	Enable to AC



* 10 Bit, 2's complement form

DISPLAY ENABLE REGISTER

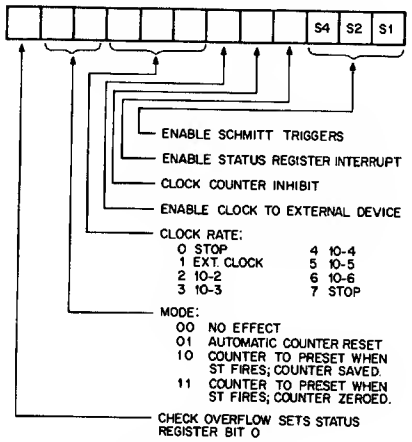


- 0—Display done flag
- 10—Display Channel
- 11—Display done causes interrupt

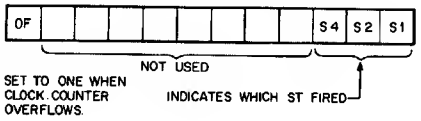
REAL TIME CLOCK (D88-EP)

CLZE	6130	One's in AC clear clock-enable register
CLSK	6131	Skip if clock overflows or ST set
CLOE	6132	One's in AC set clock-enable register
CLAB	6133	AC to buffer/ preset and counter registers
CLED	6134	Clock-enable to AC
CLSA	6135	Clock status register to AC and AC one's clear status register
CLBA	6136	Clock buffer/preset to AC
CLCA	6137	Counter register to buffer/preset and to AC

CLOCK ENABLE REGISTER



CLOCK STATUS REGISTER



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