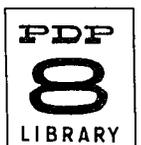


1. IDENTIFICATION

1.1 Maindec 803

1.2 PDP-8 Memory Address Test

1.3 May 11, 1965



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2. ABSTRACT

Maindec 803 provides a rough inspection of the performance of the memory address register and the decoder network which selects a given memory cell. Primarily, Maindec 803 detects errors that arise from open or shorted selection lines.

3. REQUIREMENTS

3.1 Storage

The program occupies memory cells 0001-0033. It is designed for use with the RIM Loader in locations 7756-7776. If it is used with a RIM Loader in 7700, change the contents of memory cell 0032 from 0023 to 0101 before starting the test.

3.2 Subprograms and/or Subroutines (Not Applicable)

3.3 Equipment Standard PDP-8

4. USAGE

4.1 Loading

4.1.1 Turn off the Teletype reader.

4.1.2 Set the SWITCH REGISTER to 7756; press LOAD ADDRESS, the START.

4.1.3 Place the Maindec 803 RIM program tape in the Teletype reader, and turn on the reader.

4.1.4 When the program has been loaded, stop the computer, turn off the reader, and remove the program tape.

4.2 Calling Sequence (Not Applicable)

4.3 Switch Settings

4.3.1 Starting address = 0001

4.3.2 Other settings: none

4.4 Start up and/or Entry

With the program in memory, set the SWITCH REGISTER to 0001, press LOAD ADDRESS, then START.

4.5 Errors in Usage

For any error, the following two stops occur:

Error	C(MA)	Cause of Error
E1	0017	Contents of the memory cell just inspected were incorrect. The AC displays the actual contents.
E1A	0022	The AC displays the address of the cell causing the previous error.

4.6 Recovery from such Errors

In general, the Memory Address Test detects two types of difficulty in the selection network. If a selection line is open at any point, the memory registers selectable by that line are effectively isolated from the central processor. The program is unable to write information into those cells, or read information out. Conversely, if two lines are shorted together, information entering or leaving the registers selectable by one line also enters or leaves those selectable by the other. Thus, the same information appears in two different registers.

Errors seldom occur singly. Usually, a pattern of errors appears throughout the tested portion of memory which allows the operator to isolate the possible source of trouble. The pattern usually consists of alternating blocks of erroneous and error-free memory cells. The following can be used as a guide to isolate the source of trouble.

4.6.1 If the errors occur in blocks of 100_8 registers or more, the trouble lies in the X-axis selection, and the following modules should be checked:

Module Type	Module Position	Drawing Number
G203	MC6	D8012
G203	MC7	D8012
G203	MC8	D8012
G203	MC9	D8012
G203	MD6	D8012
G203	MD7	D8012
G203	MD8	D8012
G203	MD9	D8012
G603	MP1	D8012
G603	MP2	D8012
G603	MP3	D8012
G603	MP4	D8012

4.6.2 If the errors occur in blocks of 77_8 registers or less, the trouble lies in the Y-axis selection, and the following modules should be checked.

Module Type	Module Position	Drawing Number
G203	MC12	D8013
G203	MC13	D8013
G203	MC14	D8013
G203	MC15	D8013
G203	MD12	D8013
G203	MD13	D8013
G203	MD14	D8013
G203	MD15	D8013
G603	MP5	D8013
G603	MP6	D8013
G603	MP7	D8013
G603	MP8	D8013

4.6.3 After an error halt, the test is resumed by following these procedures:

Error	Recovery
E1	Record the C(AC). Press CONTINUE to reach the next halt.
E1A	Record the C(AC). Press CONTINUE to resume the test.

5. RESTRICTIONS (Not Applicable)

6. DESCRIPTION

6.1 Discussion

The program deposits in each memory register a quantity equal to the address of that register, and then reads the contents of the same register. If the deposit and read operations were successful, it continues to the next cell in sequence. After all the testable area of memory has been checked in this manner, the program returns to the beginning of that area and attempts to read the contents of each cell. If this is successful, it returns to the first procedure, depositing information and immediately reading it. The test continues to alternate these operations, first making one pass through the tested area performing the write-then-read check, then making a second, read-only pass.

If an error occurs during a write-then-read pass, the writing is suppressed for the remainder of the pass, to insure that errors further along are not obliterated.

6.2 Examples and/or Applications

Maindec 803 is useful as a rough check of the memory selection networks when performing routine maintenance tests. It can also be used to confirm an operator's suspicions if trouble occurs during the normal operation of the computer. Generally, however, troubles arising from failures in the address selection of memory read-write circuits are likely to require the attention of a field service engineer.

7. METHODS (Not Applicable)

8. FORMAT (Not Applicable)

9. EXECUTION TIME

The program will run indefinitely, taking approximately 1.3 seconds for each pass until an error is encountered or until the operator stops the computer manually.

10. PROGRAM

10.1 Core Map (None)

10.2 Dimension List(s) (None)

10.3 Macro, Parameter, and Variable Lists (None)

10.4 Program Listing

/MAINDEC 803: PDP-8 MEMORY ADDRESS TEST:

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*1
0001 7300 BGIN, CLL CLA /INITIALIZE
0002 1024 TAD C+1 /CLEVER DODGE TO INITIALIZE ADRS
0003 3033 DCA ADRS
0004 2033 A, ISZ ADRS
0005 7630 SZL CLA /WRITING THIS PASS?
0006 5011 JMP B /NO. GO READ
0007 1033 TAD ADRS /YES.
0010 3433 DCA I ADRS
0011 1433 B, TAD I ADRS /READ &COMPARE
0012 7041 CIA
0013 1033 TAD ADRS /C(ADRS)-C(C(ADRS))
0014 7650 SNA CLA /IS RESULT=0?
0015 5023 JMP C /YES. GO ON

0016 1433 SIGH, TAD I ADRS /NO
0017 7402 EI, HLT /ERROR: AC SHOWS INCORRECT WORD
0020 7320 CLA STL
0021 1033 TAD ADRS
0022 7402 EIA, HLT /AC SHOWS CORRECT ADDRESS.

0023 7260 C, CLA CMA CML /IMPLEMENTATION OF
0024 0033 AND ADRS /THE CLEVER DODGE
0025 1032 TAD CTAB /END OF PASS TEST.
0026 7640 SZA CLA /IS IT?
0027 5004 JMP A /NO, NEXT WORD
0030 7020 CML /YES, NEXT PASS
0031 5002 JMP BGIN+1

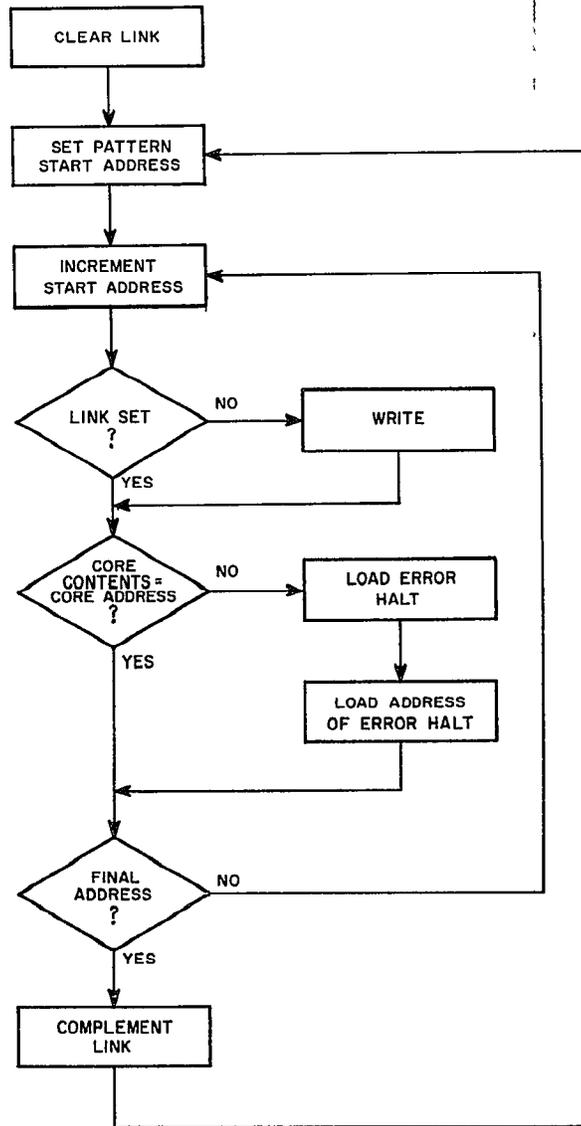
0032 0023 CTAB, 0023
0033 0000 ADRS, 0

A 0004
ADRS 0033
B 0011
BGIN 0001
C 0023
CTAB 0032
EI 0017
EIA 0022
SIGH 0016

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11. DIAGRAMS

11.1 Flow Chart



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