A607
10—Bit D/A Converter, Single Buffered

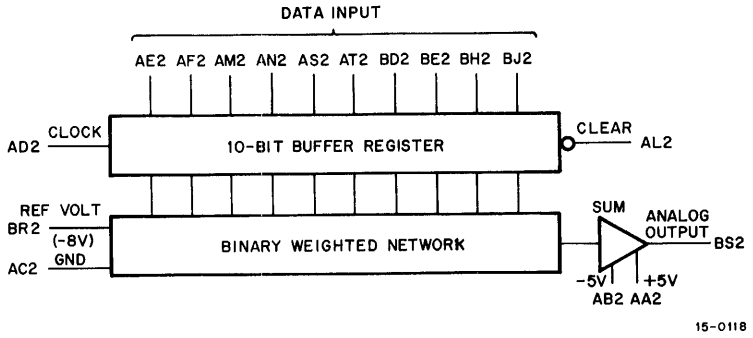
The A607 module contains a 10-bit D/A converter that consists of a 10-bit buffer register, a binary weighting network, and a current summing amplifier. The reference voltage used in the binary weighting network is externally supplied for greater efficiency and optimum scale factor matching in multi-channel applications. Data on register input lines must be settled 20 ns before the leading edge (positive-going voltage of the CLOCK pulse passes the threshold voltage and should remain stable 5 ms afterward. The duration of the positive CLOCK pulse should be at least 50 ns, and the duration of the negative CLEAR pulse should be at least 30 ns. Data present at the input of the register is transferred to the output when the leading edge of the CLOCK pulse passes the threshold. The analog output voltage is unipolar and varies from 0V to 2.0V (in two millivolt increments) in accordance with the binary input data.

The following are the input, output, and power characteristics of the A607 module.

INPUTS: Each DATA input presents one TTL unit load. The CLOCK input presents 2 unit loads, and the CLEAR input presents 3 unit loads.

OUTPUTS: The analog output voltage is capable of driving a 10 mA load (maximum).

POWER: Power dissipation of the A607 is 5V at 200 mA (maximum) and -15V at 100 mA (maximum).



A607 Simplified Diagram