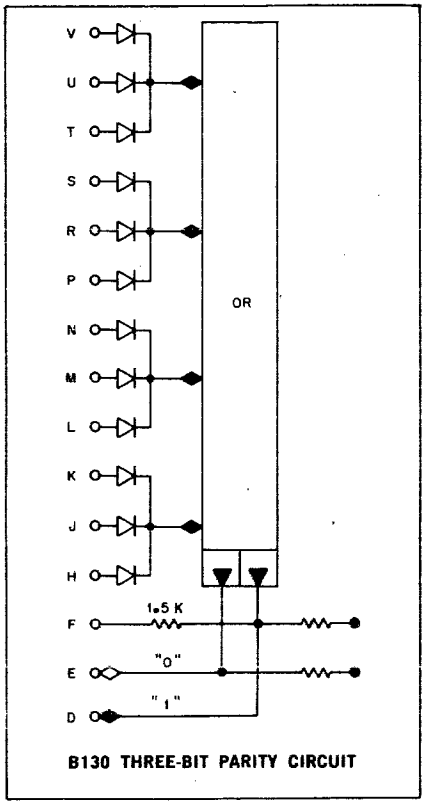
THREE-BIT PARITY CIRCUIT
TYPE B130

B SERIES



B130 THREE-BIT PARITY CIRCUIT

This special logic module has two levels of high speed logic and complementary outputs. It is designed to compute the parity (odd or even) of the contents of a flip-flop register with a minimum of time delay, but it can be used wherever there is a need for four 3-input negative diode AND gates feeding a 4-input OR gate.

Delay is typically 15 nsec from 50% of the input transition to 50% of the output transitions when output capacitive loading is very small.

INPUT: Each of the gates has a 2-ma load shared among the ground inputs of that gate. When the inputs are connected to compute parity, the total load on each of the input lines at ground is 2⅔ ma.

OUTPUT: Each of the complementary outputs can drive 10 ma at ground in addition to the built-in clamped load. The clamped loads each can drive 7 ma at −3 v. Due to the special nature of this circuit, inverter emitters may not be driven.

An indicator output is provided for applications where parity is to be displayed by an indicator-with-amplifier (4902, 4903) through an Indicator Connector Board W020.

POWER: +10 v(A)/49 ma; −15 v (B)/92 ma.

B130 — $50.00