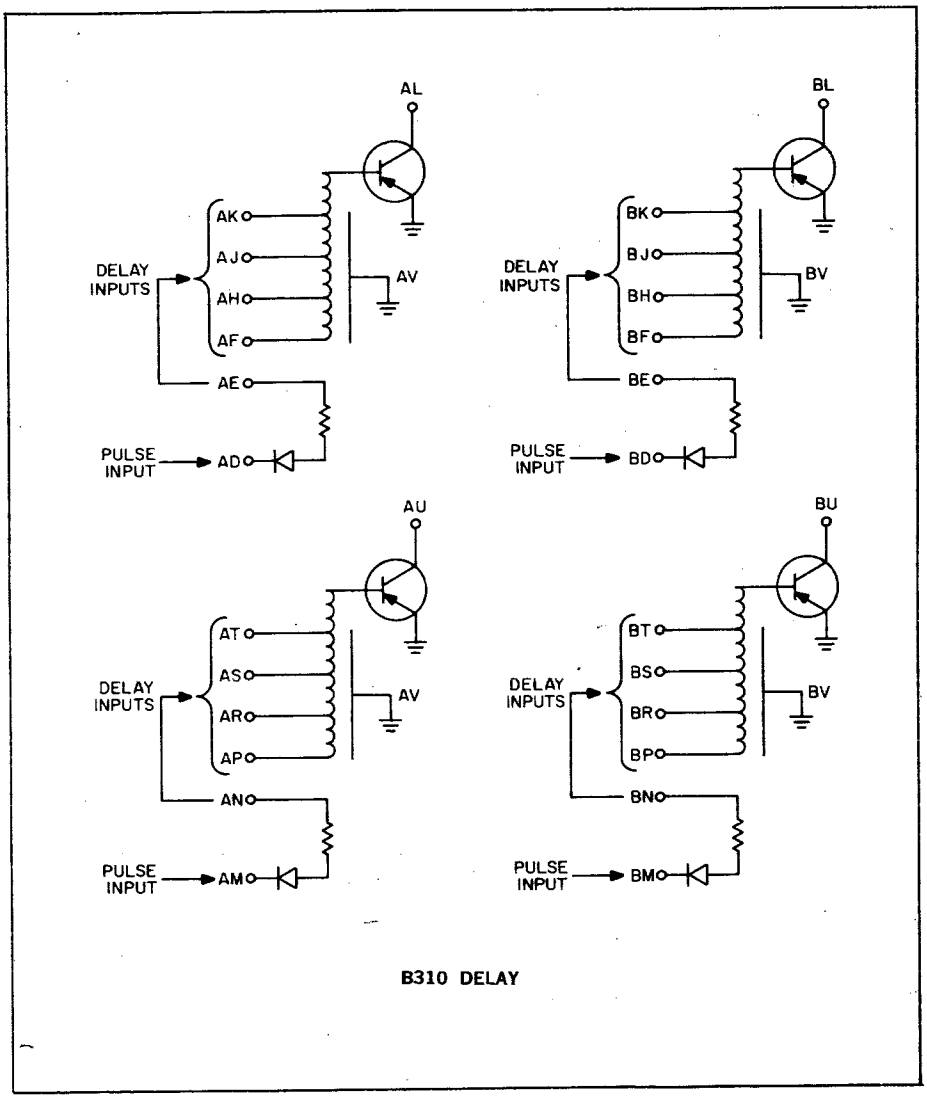
DELAY
TYPE B310
Double Height Board

B SERIES



B310 DELAY

The B310 contains four delay lines, each producing maximum delay of 50 nsec in 12.5 nsec steps. The output of each line is connected to a transistor inverter whose emitter is grounded. The collector terminal is available for logical gating. The 15 nsec delay through the inverter must be added to the delay of the line.

INPUTS: 40 nsec negative pulse or equivalent. One unit of load.

OUTPUTS: Collector should go to P.A. input of B602 or other unit being pulsed. However, up to two inverters may be placed in series between collector and P.A. input for additional logic gating.

POWER: None required.

B310 — $66.00