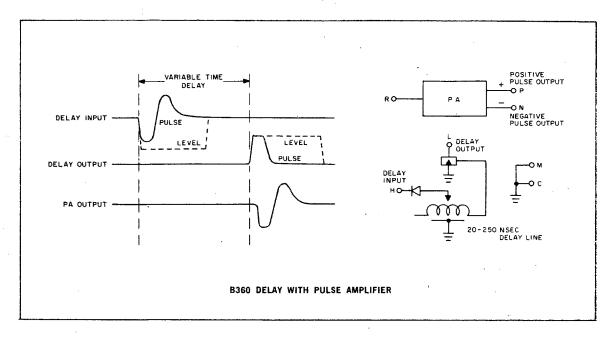
## DELAY WITH PULSE AMPLIFIER TYPE B360

## B



The B360 contains a delay line which may be varied from 25 nsec to 250 nsec, and a standardizing pulse amplifier similar to one half of a B602. The length of the delay is adjusted by means of a slotted screw accessible from the handle-end of the module. The high resolution of the delay line (approximately ¼ nsec) makes it ideal for high-speed timing chains. By connecting the delay and pulse amplifier together with suitable logic in a feedback loop, a stable gateable clock may be obtained (see Application Section).

**INPUT:** Delay — Pulse — The pulse input to the delay is a standard 40-nsec 2.5-v negative pulse. Loading is equivalent to four inverter bases. Level — The static input load is 12.50 ma at —3 v. Dynamic load is negligible. The input may be driven by three W005 Clamped Loads in parallel, or by one W005 Load in parallel with a standard 10-ma clamped load.

**Pulse Amplifier** — The input of the pulse amplifier is equivalent to a 10-ma clamped load, and is driven by an inverter. **Pulse** — At the base of the inverter the pulse input which drives the pulse amplifier, is normally a standard 40-nsec negative pulse. However, any negative pulse having an amplitude between 2 and 5 v, a rate of change greater than 1 v/12 nsec and width (at —2 v) greater than 25 nsec, can be used instead of the 40-nsec pulse. Inverter input

pulses of less than -0.5 v will not generate an output pulse. **Level** — The input to the pulse amplifier may also be a standard positive-going level change (-3 v to ground). A negative-going level change will not produce an output signal from the amplifier. The input must have been at -3 v for at least 50 nsec before going to ground.

**OUTPUT: Delay** — **Pulse** — When the input of the delay line is a 40-nsec pulse, the maximum output driving capacity at ground is 16 ma as with a standard inverter driven by a pulse. **Level** — When the input to the delay is at level, the maxmium output driving capability at ground is 36 ma as with the output transistors of a buffered flip-flop. Each 10-ma clamped load attached to the output (collector) provides a maximum output driving capacity of 7 ma at —3 v. The dynamic load of the collector is 8 pf.

Pulse Amplifier — The output of the pulse amplifier (for either a negative pulse or a negative-going level change at the base of the inverter driving the amplifier) is a standard 2.5-v 40-nsec pulse which occurs at the output terminal every time the input signal meets the input requirements. The negative output will be activated if the positive output terminal is grounded. Each output drives twelve 10-mc bases and appropriate terminating resistors.

**POWER:** +10 v(A)/5 ma; -15 v(B)/50 ma.