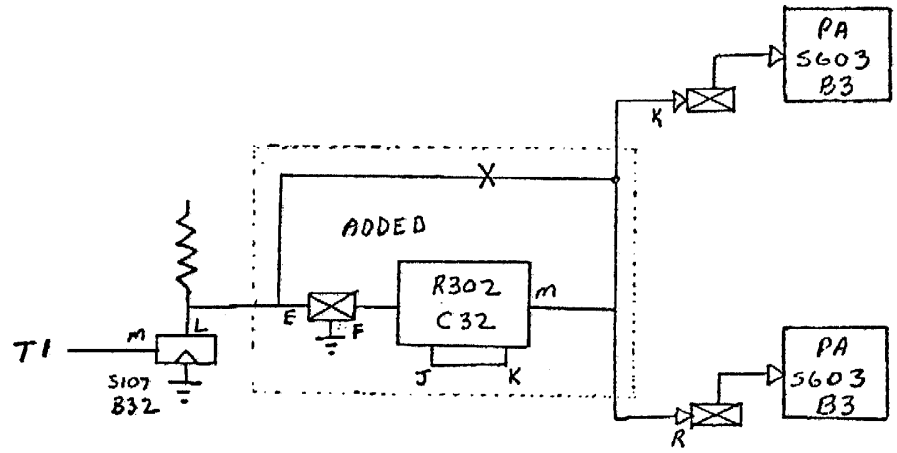
Title	INTERMITTENT DATA ERRORS		Tech Tip Number
All	Processor Applicability: 8I 8L	Author R. Woodson Rev A Approval Date 9-30-74	Cross Reference

SYMPTOMS: When running DEC-X8 or any other program that causes back to back breaks of 3 cycle and single cycle devices, data errors occur on single cycle device.

SOLUTION: Modify DM01 as shown below.



To adjust R302 for best operation pin M of the R302 should be initially set to rise to ground level at the leading edge of TS3 in the processor. Then a pattern of all ones should be written on a data break device (preferably a disk for scoping) to be read back during adjust ment. Tod adjust get computer in loop reading back all ones pattern written earlier. While syncing on break (1) look at data out of an adder and MB load. MB load, the first one on sweep, should occur during the time a one (low) is coming out of the adder. The R302 should now be adjusted until the leading edge of MB load falls approx. 50 ns before the trailing edge of the one.

Routines for writing and reading all ones should be available in the devices diagnostics.