Slice Level: Variable between 0 and -11.6 Vdc with respect to +10 Vdc.

4.3 G010 SENSE AMPLIFIER SELECTOR

This module contains two noninverting driver circuits. Using standard input levels, each drive circuit can drive a large number of base loads and diode loads with levels of -3V and -6V. Refer to Figure 4-3 for the module block diagram.

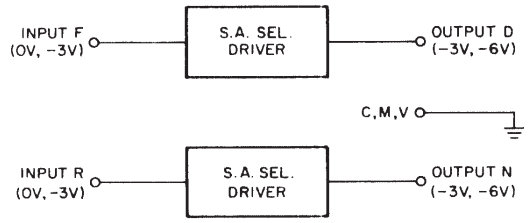

Figure 4-3 Sense Amplifier Selector

Input: Standard DEC logic levels are used; 2 mA of base load are used when the input is -3 Vdc.

Output: A -3 Vdc level occurs when the input level is at ground; a -6 Vdc level occurs when the input level is at -3 Vdc. These levels can drive ±40 mA at 10 Mc. Drive delay is approximately 40 ns.

4.4 G206 MEMORY SELECTOR

This module is used as a selector switch in the read/write matrix of coincident current memories. Refer to Figure 4-4 for the following functional description. Each module contains two read gates and two write gates. Due to the decoding, only one read gate and one write gate may be enabled at one time. Although this module is primarily intended for four-bit decoding, it may be used for three-bit decoding by grounding pin AK.

Input: Standard DEC -3 Vdc levels are used for turn on. The decoding gates and the LSB gate draw one unit of base current. The read or write gates draw two units of base current.

Output: Each output can drive 425 mA for 500 ns at a PRF of 1 MHz. The following specifications refer to the output waveform.

Maximum delay for output fall: 80 ns

Maximum delay for output rise: 50 ns

Minimum cycle time: 1.3 μs

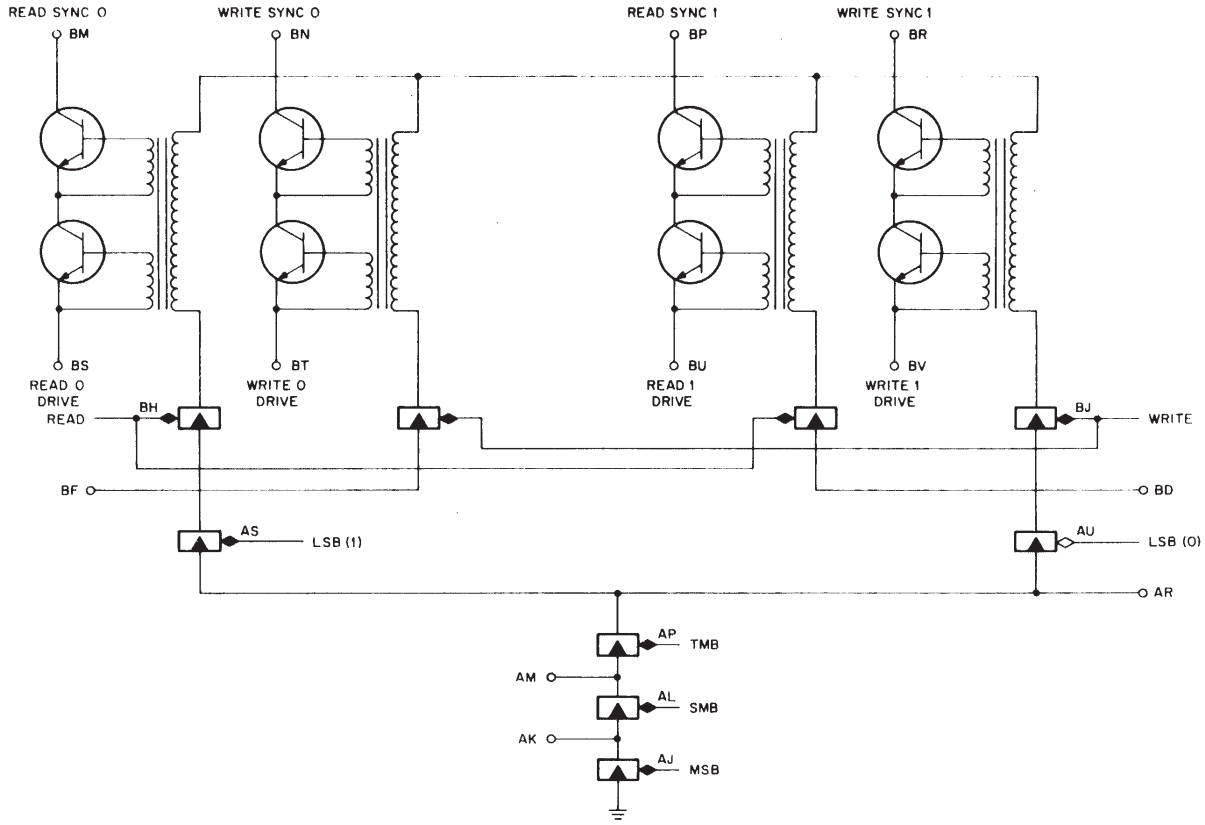

Figure 4-4 G206 Memory Selector

4.5 G207 INHIBIT DRIVE

This module is used to drive the inhibit winding of magnetic core memory planes. Refer to Figure 4-5 for the following functional description. Each module contains four identical gated circuits. A balun (1/1 balanced trap) at the output is used to obtain balanced drive. The switched current is determined by the inhibit resistor.

Input: Standard DEC -3 Vdc levels are used for turn on. The quadrant selection gates draw two units of base current and the MB gate-input draws three units of base current. Each of the inhibit gate inputs draws 1 unit of base current.

Output: Each output can drive 350 mA for 600 ns at a PRF of 750 KHz. The following specifications refer to the output pulse.

Maximum delay for output fall: 60 ns

Maximum delay for output rise: 60 ns

Minimum cycle time: 1.3 μs