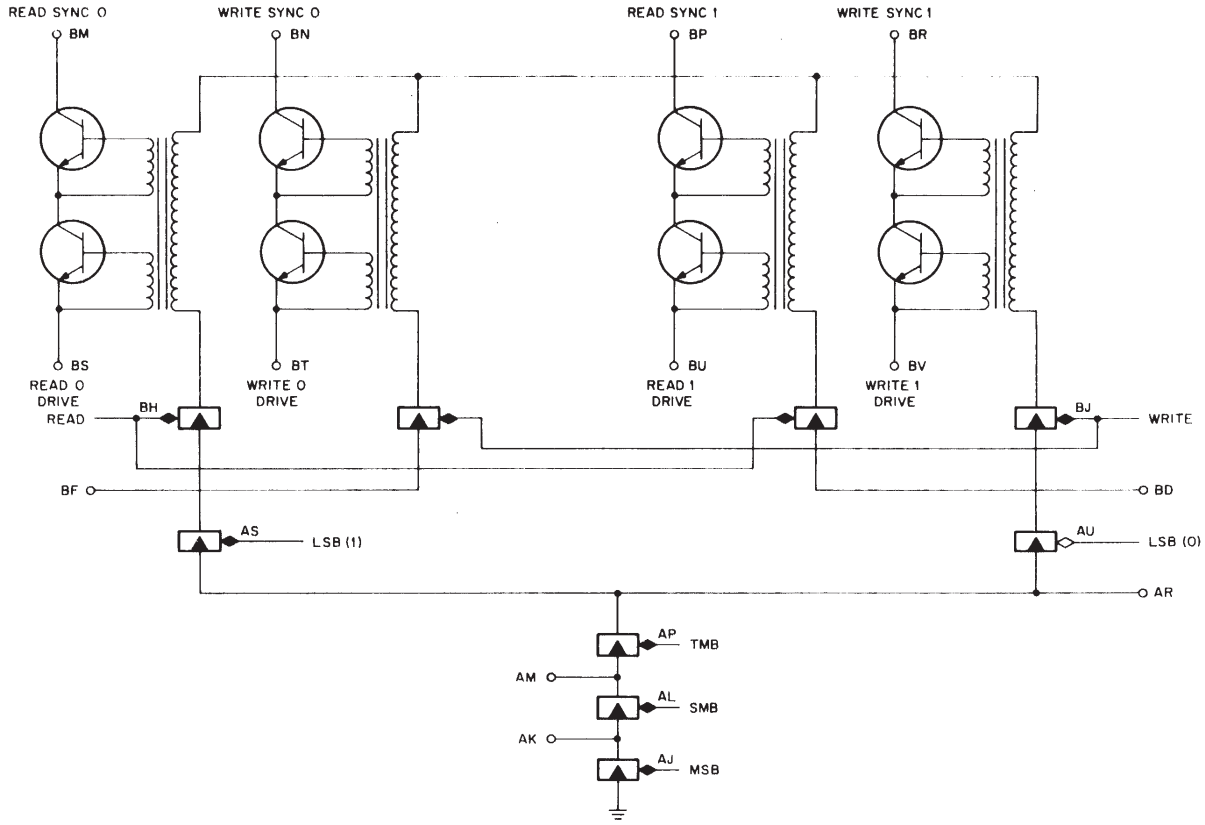

Figure 4-4 G206 Memory Selector

4.5 G207 INHIBIT DRIVE

This module is used to drive the inhibit winding of magnetic core memory planes. Refer to Figure 4-5 for the following functional description. Each module contains four identical gated circuits. A balun (1/1 balanced trap) at the output is used to obtain balanced drive. The switched current is determined by the inhibit resistor.

Input: Standard DEC -3 Vdc levels are used for turn on. The quadrant selection gates draw two units of base current and the MB gate-input draws three units of base current. Each of the inhibit gate inputs draws 1 unit of base current.

Output: Each output can drive 350 mA for 600 ns at a PRF of 750 KHz. The following specifications refer to the output pulse.

Maximum delay for output fall: 60 ns

Maximum delay for output rise: 60 ns

Minimum cycle time: 1.3 μs

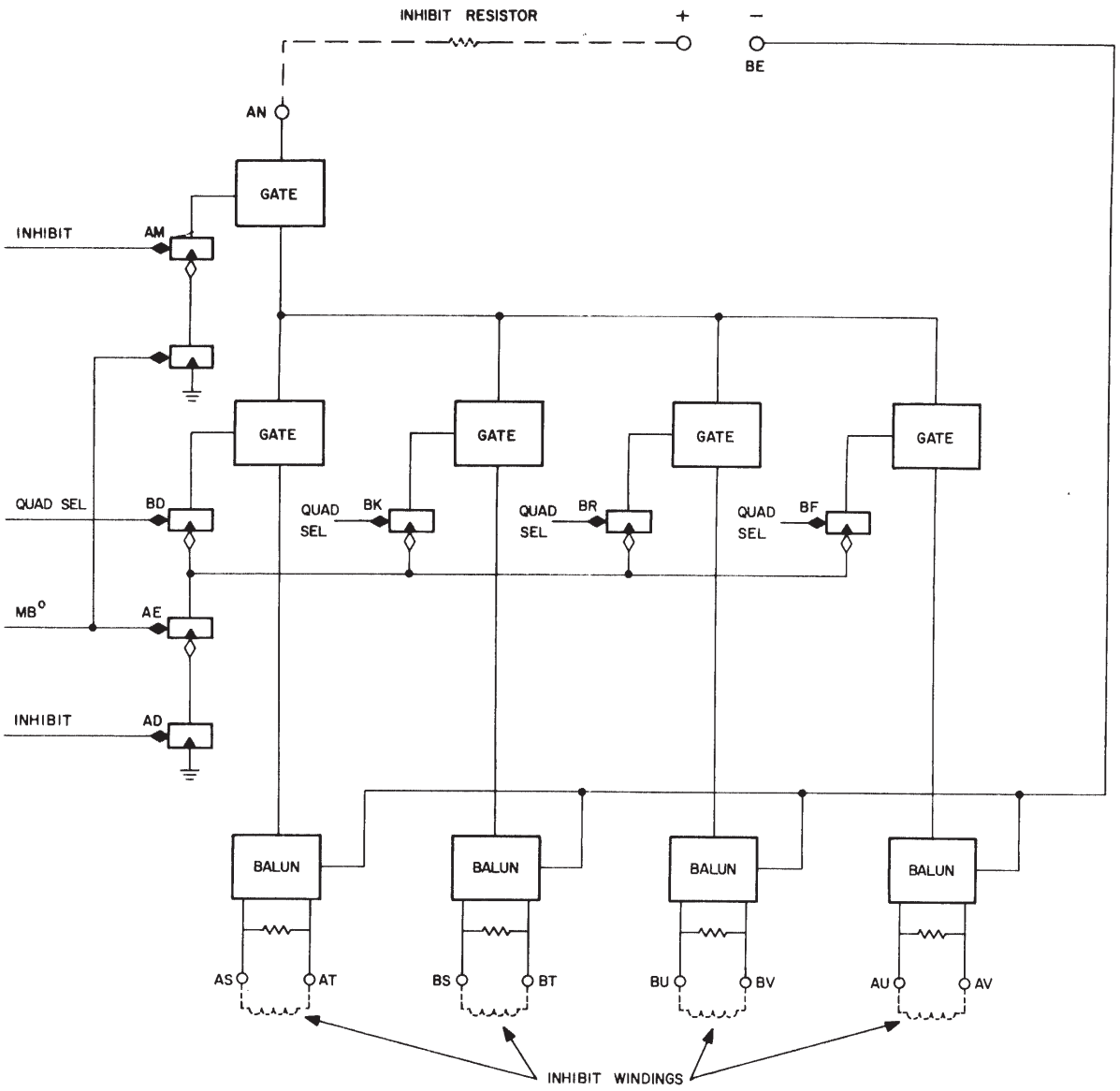

Figure 4-5 Inhibit Drive

4.6 G212 MEMORY COMMON DRIVE

This double height module is used as a common drive in the read/write matrix of coincident current memories. Refer to Figure 4-6 for the following functional description. Each module contains two read gates and two write gates but the decoding gate enables only one read gate and one write gate at a time. The decoding circuit is used to decode a 4-bit address. Clamping diodes are connected to terminals AE and AF to limit transients, and compensating resistors are connected to terminals BE and BK to bias the diode balun matrix.