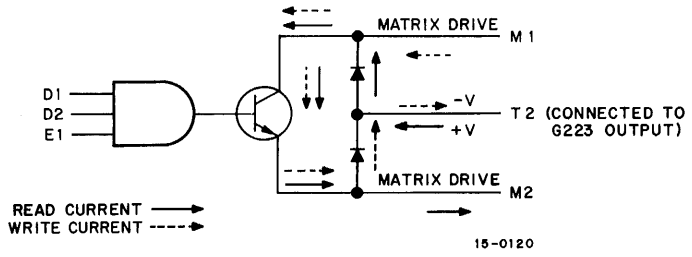
G222
Memory Selector

The G222 module contains four memory selectors. Eight of these modules are used in the PDP-15 for each 4K memory stack. (Refer to Engineering Drawings D-BS-MM15-0-6 and D-BS-MM15-0-7.) The modules are used to decode the memory address to obtain the X- and Y-axis select signals for accessing the core memory. Each memory selector consists of a 3-input NAND gate and a bidirectional current switch network for both read and write current. An 8 x 8 matrix (see G613 and G614) is used for each of the X and Y selection paths. Thus, two switches must be energized to establish the path in the X plane, and another two switches must be energized to establish the path in the Y plane. In a 4K system a total of four G222 modules are used to decode the first six bits of the memory address. This provides one out of 64 states for the Y plane. Similarly, four G222 modules are used to decode the remaining six bits of the memory address in order to establish the selection path in the X plane.



G222 Simplified Diagram

The following are the input and output characteristics of the G222 modules.

INPUTS: Each NAND gate input presents 2.5 TTL unit loads.

OUTPUTS: Each matrix selector switch handles 400 mA (typical).