3.4.5 Read Operation

When the section of tape shown in Figure 3-5C is read, the relative positions of the timing and data track flux reversals ensure that the two signals will be read back 90 degrees out of phase. Therefore, if the tape is read while moving in the same direction as it was written, (i.e., the tape was written, rewound over the head, and read), the TP1 pulses will occur close to maxima of the signals from the data tracks.

In order to read the tape, the signals from the data amplifiers are fed to the inputs of the data buffer, and loaded into the buffer when TP1 occurs.

Figure 3-5A illustrates the timing track, TP0, TP1, and data track 0 signals which are generated when the section of tape shown in Figure 3-5C is read while moving in the same direction as it was written. Note that each TP1 pulse occurs at a maximum of the data track signal, and that the polarity of the data track signal at that time defines the value of the bit that was recorded there.

3.5 MODULE DESCRIPTION

Circuit information for the FLIP CHIP modules used in the TU56 DECtape Transport is cataloged in the DEC *Digital Logic Handbook,* C-105. Schematics of these and noncataloged modules are contained in Appendix A. The following paragraphs describe only the noncataloged modules.

3.5.1 G847 Dual Motor Voltage Control

The G847 Dual Motor Voltage Control module (Drawing B-CS-G847-0-1) selects the voltage level that is applied to the tape reel motors. This module contains two 3-stage circuits for control of the two reel motors.

When the run signal is high, Q1 is biased on. Q2 and Q3 are then, in turn, biased on. With Q3 conducting, a high output voltage (approximately +38V) appears at Eout 1. Diode D4 is then reverse biased following the higher output voltage.

Diodes D2 and D9 ensure that the potentials at the base of Q3 and the collector of Q2 do not exceed their design ratings.

When the run signal is low, Q1, Q2, and Q3 are off and D4 conducts; thus, the lower voltage (approximately +18V) appears at Eout 1. Eout 1 is at +38V during run and brake time and at +18V when drag is required on a particular motor. Eout 1 is also at +18V when the REMOTE/OFF/LOCAL switch (SW2) is in the OFF position.

3.5.2 G848 Motor Control Module

The G848 Motor Control module (Drawing C-CS-G848-0-1) is a transistorized bridge circuit designed to operate an ac tape reel motor from a dc source. The operational ac is obtained from an external 40-Hz clock oscillator, whose OSC0 and OSC1 outputs are 180 degrees out of phase with each other.

The bridge circuit controlling the ac tape motor consists of two PNP transistors (Q5 and Q8) and two NPN transistors (Q6 and Q7). The OFF signal can remove power from the motor for an indefinite period.

Transistor turn-on, RC time delay networks (R15 and C4; R24 and C3; R23 and C2; and R3 and C1) prevent two opposing arms in the bridge network from being biased on at the same time. The time delay from turn-off to turn-on is approximately 1 millisecond.

When the OSC1 input is high, Q11 is biased on, and C2 discharges through the low impedance path of the transistor to ground. When C2 discharges, Q10 turns off. When C4 has sufficiently discharged through D12, R15, and Q11, Q9 is turned on and provides a path from the motor power supply to the base of Q7, turning Q7 on.

When the OSC1 input is high, the OSC0 input is low, biasing Q2 off. C1 charges through R3, which in turn causes Q3 to be turned on. Once Q3 is biased on, it turns Q5 on. Diode D8 is then reverse biased, Q4 is biased off, and C3 charges through R25. A current path now exists from the motor power supply, through Q5, through the motor windings, and through Q7 to ground.

The opposite operational characteristics occur when OSC1 input goes low and OSC0 goes high. For this change of state, Q11, Q9, Q7, Q5, and Q3 are now reverse biased, and Q2, Q4, Q6, Q8, and Q10 are forward biased. The two halves of the bridge network oscillate at the 40-Hz clock rate, generating ac current through the motor winding and inducing motor motion.

3.5.3 G859 Clock Regulator Module

The G859 Clock Regulator module (Drawing B-CS-G859-0-1) contains a divide-by-two flip-flop (Q6 and Q7), an 80-Hz oscillator (Q2 and Q3), and a voltage regulator (Q5). The 80-Hz oscillator output is fed through capacitors C3 and C4 to the flip-flop. The resulting 40-Hz square wave output is then connected through two emitter followers (Q1 and Q4) to the G848 Motor Control module.

NOTE

During tape motion, the high harmonic content of the 40-Hz square wave that supplies the tape reel motors produces small, cyclic variations in the power output of the motors. These variations may cause an audible hum which varies in intensity as the reel being driven by a particular motor fills with tape. Such behavior is normal, and has no effect on the performance of the transport.

When +10V is connected to pin A2 of this module, the +5V regulator circuit reduces this input voltage to the +5V level required for logic operation. If +5V is available from an external power supply, the regulator circuit is bypassed.

3.5.4 G888 Manchester Reader/Writer Module

The G888 module (Drawing B-CS-G888-0-1) consists of two portions. The upper read portion of the schematic contains the following:

a. a linear amplifier (E1) with a gain of 100
b. a zero-crossing detector (E2)
c. a limiter (Q1)

During a read operation, the 10 to 12 mV read signals from the read head are applied to pins D and E of linear amplifier E1. The approximately 1V amplified output (test pin H2) is then transmitted to zero-crossing detector E2 pin 2. The square wave E2 output is clamped, by limiter Q1, to the standard DEC logic levels and applied to output gate E3. The signal at output pins U and V is then transmitted via the interface lines to the controller read/write buffer.