When the OSC1 input is high, Q11 is biased on, and C2 discharges through the low impedance path of the transistor to ground. When C2 discharges, Q10 turns off. When C4 has sufficiently discharged through D12, R15, and Q11, Q9 is turned on and provides a path from the motor power supply to the base of Q7, turning Q7 on.

When the OSC1 input is high, the OSC0 input is low, biasing Q2 off. C1 charges through R3, which in turn causes Q3 to be turned on. Once Q3 is biased on, it turns Q5 on. Diode D8 is then reverse biased, Q4 is biased off, and C3 charges through R25. A current path now exists from the motor power supply, through Q5, through the motor windings, and through Q7 to ground.

The opposite operational characteristics occur when OSC1 input goes low and OSC0 goes high. For this change of state, Q11, Q9, Q7, Q5, and Q3 are now reverse biased, and Q2, Q4, Q6, Q8, and Q10 are forward biased. The two halves of the bridge network oscillate at the 40-Hz clock rate, generating ac current through the motor winding and inducing motor motion.

3.5.3 G859 Clock Regulator Module

The G859 Clock Regulator module (Drawing B-CS-G859-0-1) contains a divide-by-two flip-flop (Q6 and Q7), an 80-Hz oscillator (Q2 and Q3), and a voltage regulator (Q5). The 80-Hz oscillator output is fed through capacitors C3 and C4 to the flip-flop. The resulting 40-Hz square wave output is then connected through two emitter followers (Q1 and Q4) to the G848 Motor Control module.

NOTE

During tape motion, the high harmonic content of the 40-Hz square wave that supplies the tape reel motors produces small, cyclic variations in the power output of the motors. These variations may cause an audible hum which varies in intensity as the reel being driven by a particular motor fills with tape. Such behavior is normal, and has no effect on the performance of the transport.

When +10V is connected to pin A2 of this module, the +5V regulator circuit reduces this input voltage to the +5V level required for logic operation. If +5V is available from an external power supply, the regulator circuit is bypassed.

3.5.4 G888 Manchester Reader/Writer Module

The G888 module (Drawing B-CS-G888-0-1) consists of two portions. The upper read portion of the schematic contains the following:

a. a linear amplifier (E1) with a gain of 100
b. a zero-crossing detector (E2)
c. a limiter (Q1)

During a read operation, the 10 to 12 mV read signals from the read head are applied to pins D and E of linear amplifier E1. The approximately 1V amplified output (test pin H2) is then transmitted to zero-crossing detector E2 pin 2. The square wave E2 output is clamped, by limiter Q1, to the standard DEC logic levels and applied to output gate E3. The signal at output pins U and V is then transmitted via the interface lines to the controller read/write buffer.

The lower write portion of the schematic contains a push-pull amplifier (Q3 and Q5). During a write operation, write data from the controller is ANDed with the T/M ENAB signal at input gate E3 pins 9, 10, 12, and 13. Either output pin J or K, depending upon the polarity of the input signal, drives current to the read/write heads. The applicable G888 module specifications are as follows:

Write Amplifier

Inputs:	Standard TTL voltage. Load at 0V is 1 unit. R2 should be tied to +3V when not used.
Outputs:	Can drive 100 mA in either direction. Pins L2 and M2 are the outputs of the 7400 TTL gates. Pins J2 and K2 are the outputs that drive the tape unit write head.

Read Amplifier

Inputs:	Can detect an input voltage as low as 500 μV.
Outputs:	Pins U and V are standard TTL voltages.
Fan Out:	Pin U2 = 9 unit loads Pin V2 = 10 unit loads
Test Point:	Pin H2 is a test point for the first stage output.

Power Dissipation	50 mW at +5V 250 mW at -15V