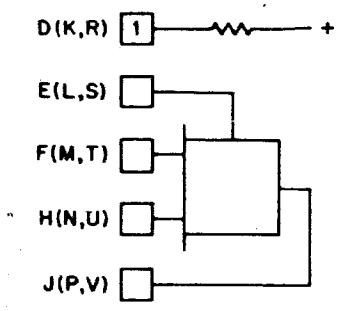
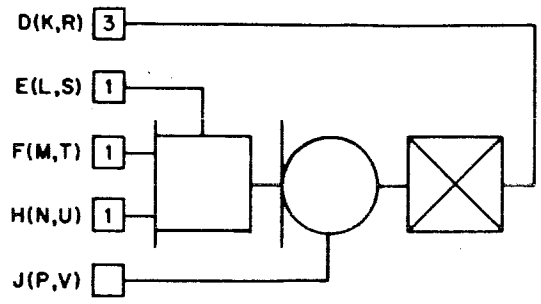
AND/OR GATES

TYPES K003, K113, K123

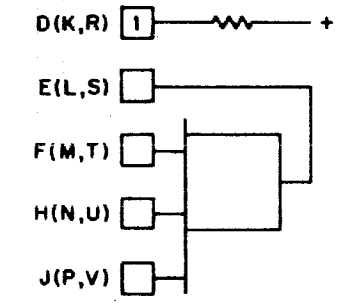
K SERIES



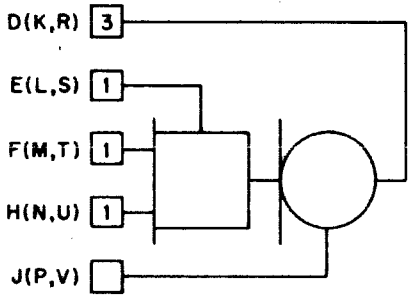
AND for OR expansion



AND/NOR



AND for AND expansion

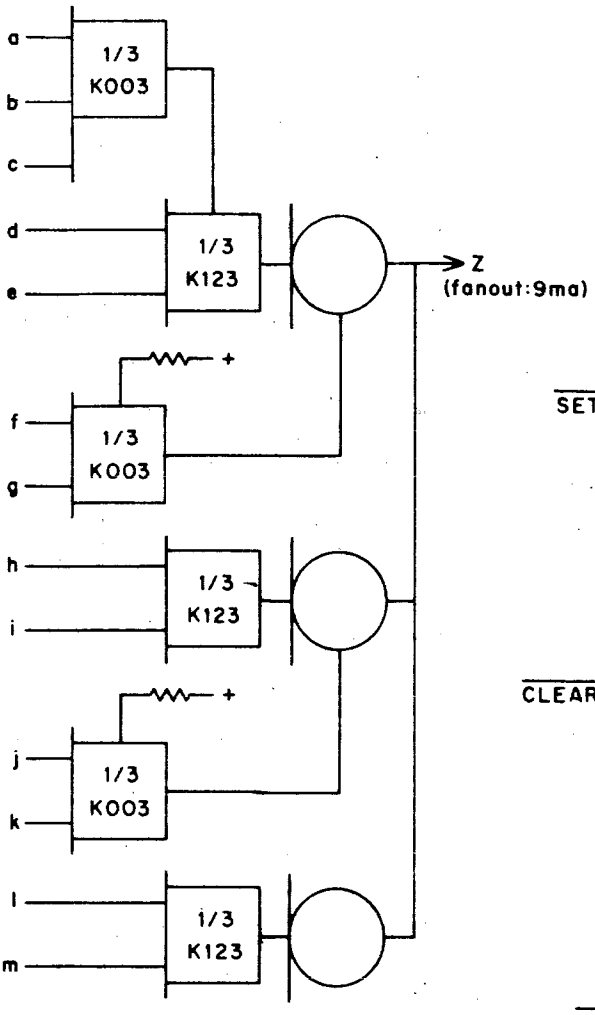


AND/OR

Module Type	K003	K113	K123
Function	Expander	Inverting Gate	English Gate
Per Module	3	3	3
Fanout	15	15	15
Slow Connection	B → D	B → D	B → D
Slowed Points	D	D	D

Any logical decision may be performed with these three elements. For NOR logic, K123 is not needed. For English logic, K113 provides NOT elements. Outputs may be tied together to obtain more gating. The example below shows one K123, plus one K003, connected to form the English expression: z = [(a AND b AND c AND d AND e) OR (f AND g)] AND [(h AND i) OR (j AND k)] AND [l AND m].

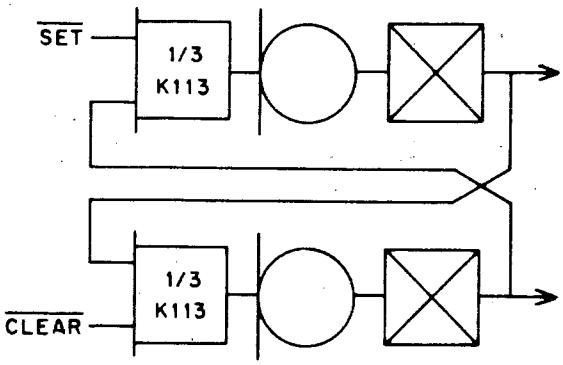
In Boolean algebra the expression reads: $z = (abcde + fg)\ (hi + jk)\ (lm)$.



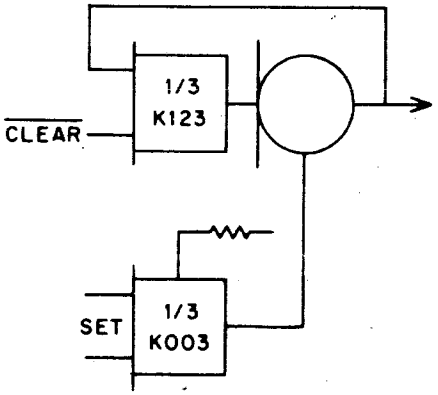
NOTE: Non-inverting K123 outputs can be connected together to provide a wired AND.

Inverting K113 outputs can be connected together to provide a wired OR.

Two kinds of control flip-flops made from logic gates are shown below.



Flip-flop 1



Flip-flop 2

Flip-flop 1: This flip-flop is reset when output B is at logic 1 and output A is at logic 0. The flip-flop sets (A = 1, B = 0), when the SET input is brought to logic 0. The flip-flop resets, when the CLEAR input is brought to logic 0. In the quiscent state, both the SET and CLEAR inputs must be held at logic 1.

Flip-flop 2: This flip-flop is reset when output A is at logic 0. The flip-flop sets when both the SET 1 and SET 2 inputs are brought to logic 1. The flip-flop resets when the CLEAR input is brought to logic 0. In the quiscent state, either SET 1 or SET 2 must be at logic 0 and the CLEAR input at logic 1.

K003 — $ 4.00
K113 — $11.00
K123 — $12.00