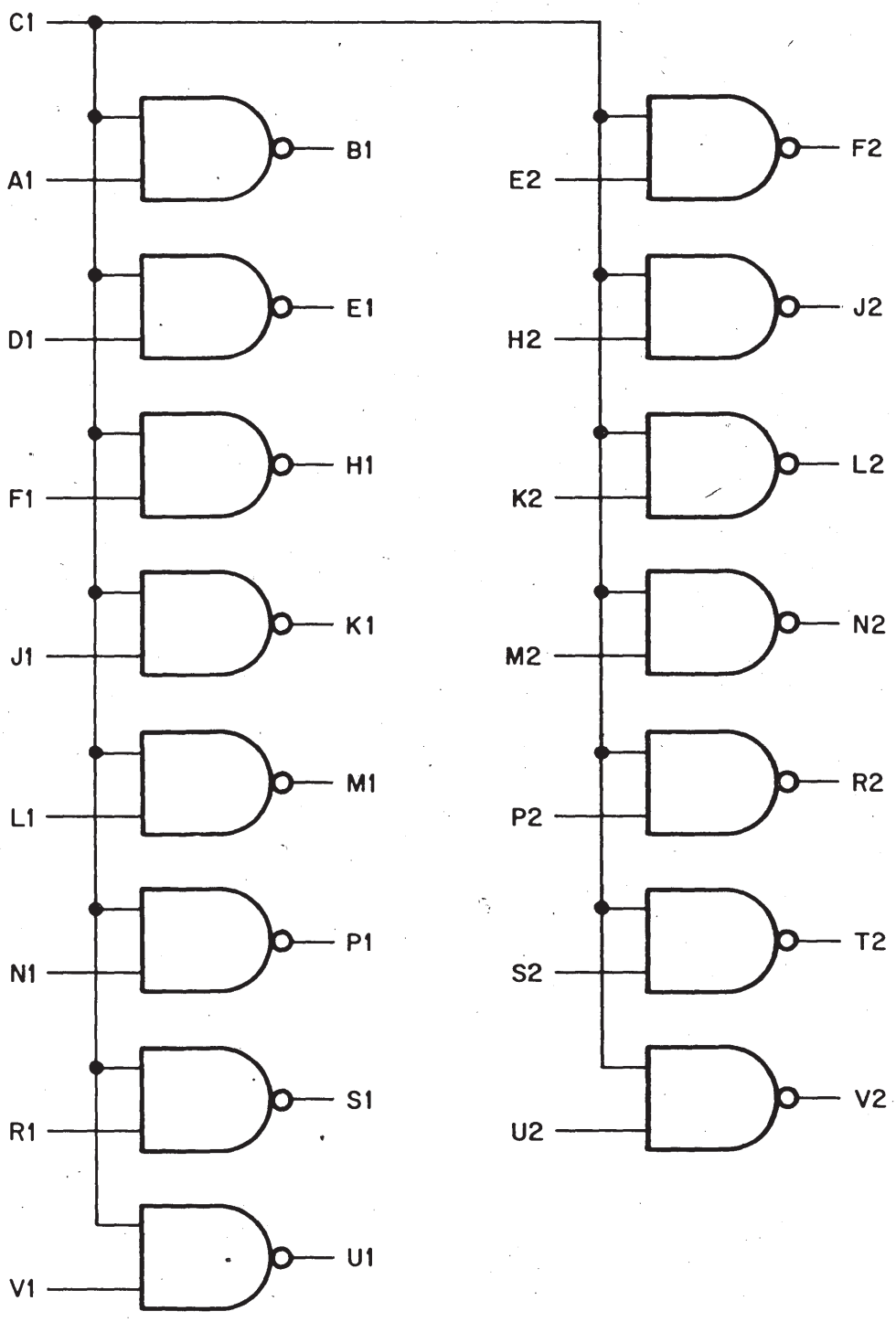
BUS DATA INTERFACE
M101

M SERIES



POWER

← A2 — +5V

← C2, T1 — GRD

The M101 contains fifteen, two-input NAND gates arranged for convenient data strobing off of the PDP8/I or PDP8/L positive bus. One input of each gate is tied to a common line so that all data signals on the second input of each gate can be enabled simultaneously. The M101 can also be used as inverters or a data multiplexer. All data inputs are protected from a negative of more than —0.8 volts.

Inputs: Each data signal input presents one TTL unit load. The common line input presents fifteen unit loads.

Outputs: Each output can drive ten unit loads.

Power: +5V at 82 ma. (max.)

M101—$24