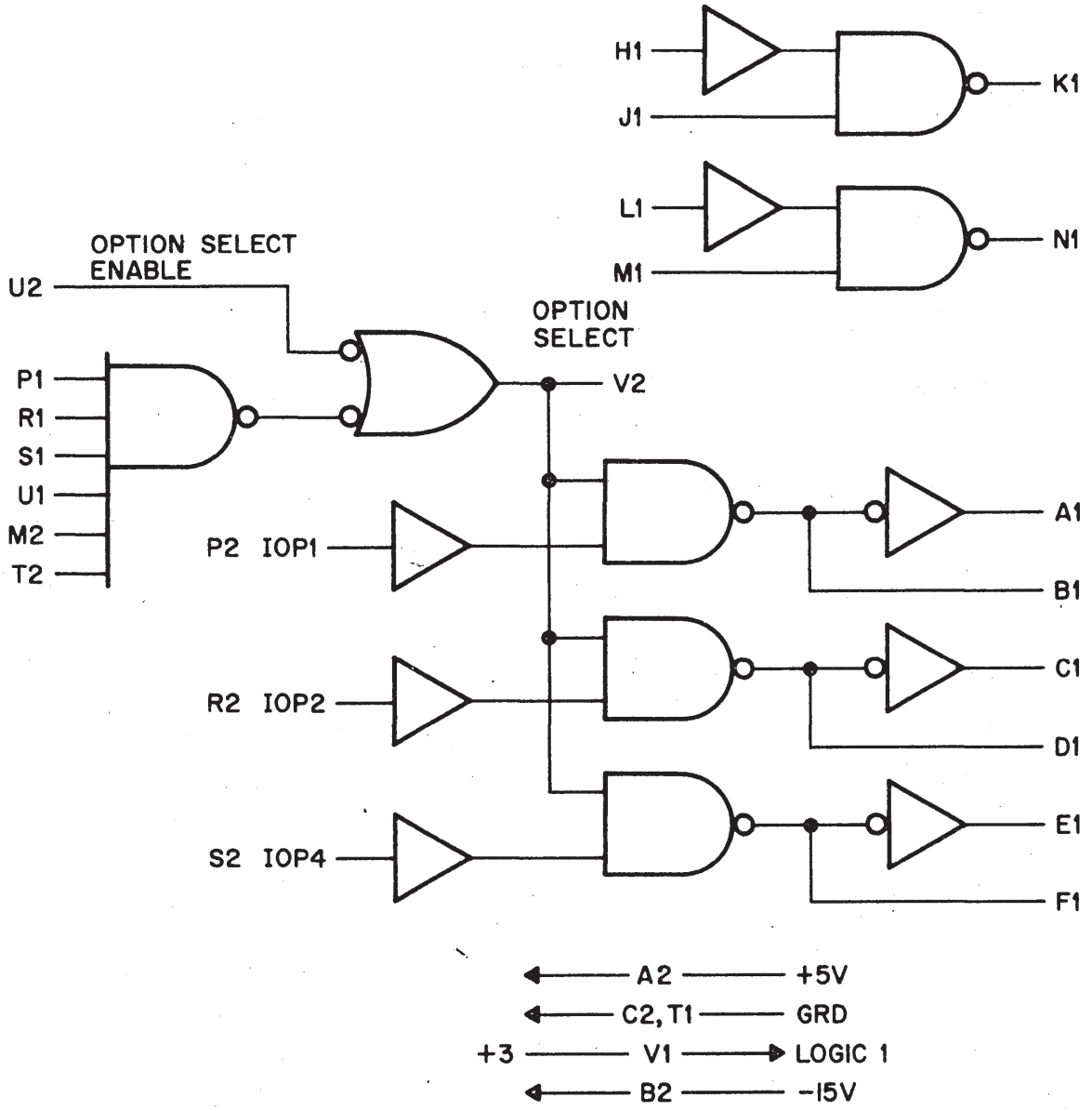
DEVICE SELECTOR
M102

M SERIES



The M102 is used to decode the six device address bits transmitted in complementary pairs on the negative bus of the PDP-8, PDP-8/I. The outputs of the M102 are compatible with M Series TTL logic. The M102 is pin compatible with the M103 Positive bus device selector with the exception of the address inputs. The true state of the BMB outputs of the PDP-8 and PDP-8/I are defined as ground where the true states of the PDP-8/I positive bus and PDP-8/L are defined as an active voltage state. This fact requires that the complement of the address bits used for an M103 must be connected to the M102.

As the address complement is tied to the pins D2, E2, F2, H2, J2, K2, an M103 may be directly substituted for an M102 when changing from a negative to a positive bus.

Inputs: U2 represents 1.25 TTL unit loads, J1, M1 represents 1 TTL, P1, R1, S1, U1, M2 and T2 standard levels of −3 volt and ground. Input load is 1 ma. shared among the inputs that are at ground.

P2, R2, S2, H1 and L1
0.2 ma. when V in = 0v
0.0 ma. when V in = −3v
Propagation Delay 40 nsec typ.

Outputs: K1 and M1 can drive 10 TTL unit loads. A1, B1, C1, D1, E1, F1 can each drive 37 TTL unit loads. U2 can drive 16 TTL unit loads.

Conversion: Logic Diagram. An active voltage is a True State, i.e., −3v or +3v = "1". A ground is a True State.

Power: +5 volts at 130 ma. (max.); −15 volts at 40 ma. (max.)

M102 — $60