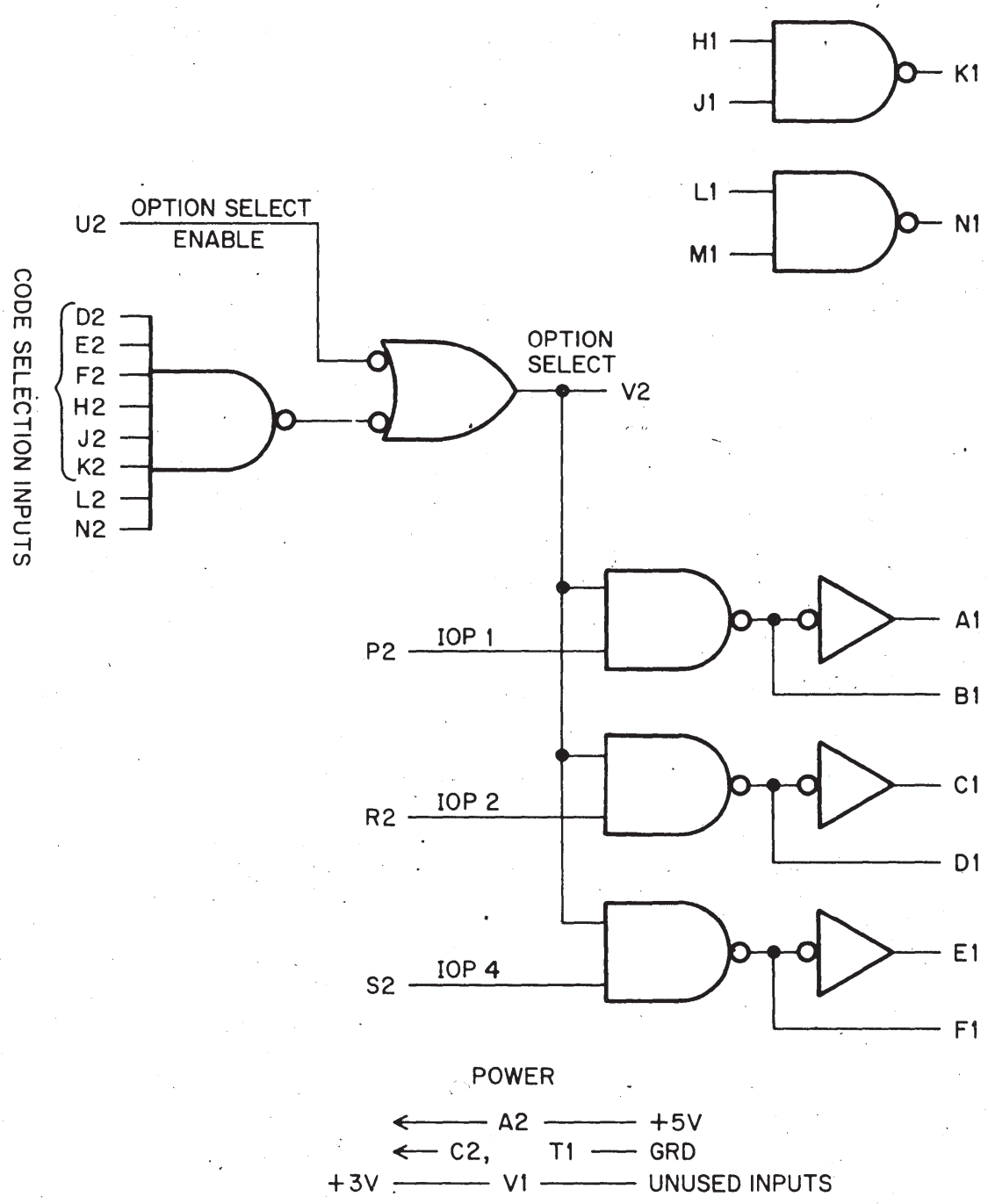
DEVICE SELECTOR
M103

M SERIES



The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

Inputs: All inputs which receive positive bus signals are protected from negative voltage undershoot of more than —0.8V.

The following inputs each present one TTL unit load D2, E2, F2, H2, J2, K2 H1, J1, L1, and M1. Inputs P2, R2, and S2 present 2.5 TTL unit loads. Inputs U2, L2 and N2 each present 1.25 unit loads. These inputs need not be tied to a source of logic 1 when not used.

Outputs: Gate outputs K1 and N1 can each drive ten TTL unit loads.

Pulse buffering outputs A1, B1, C1, D1, E1 and F1 can each drive 37 TTL unit loads.

The Option Select output can drive 16 TTL unit loads.

Power: +5 volts at 110 ma. (max.)

M103—$50