M105
ADDRESS SELECTOR

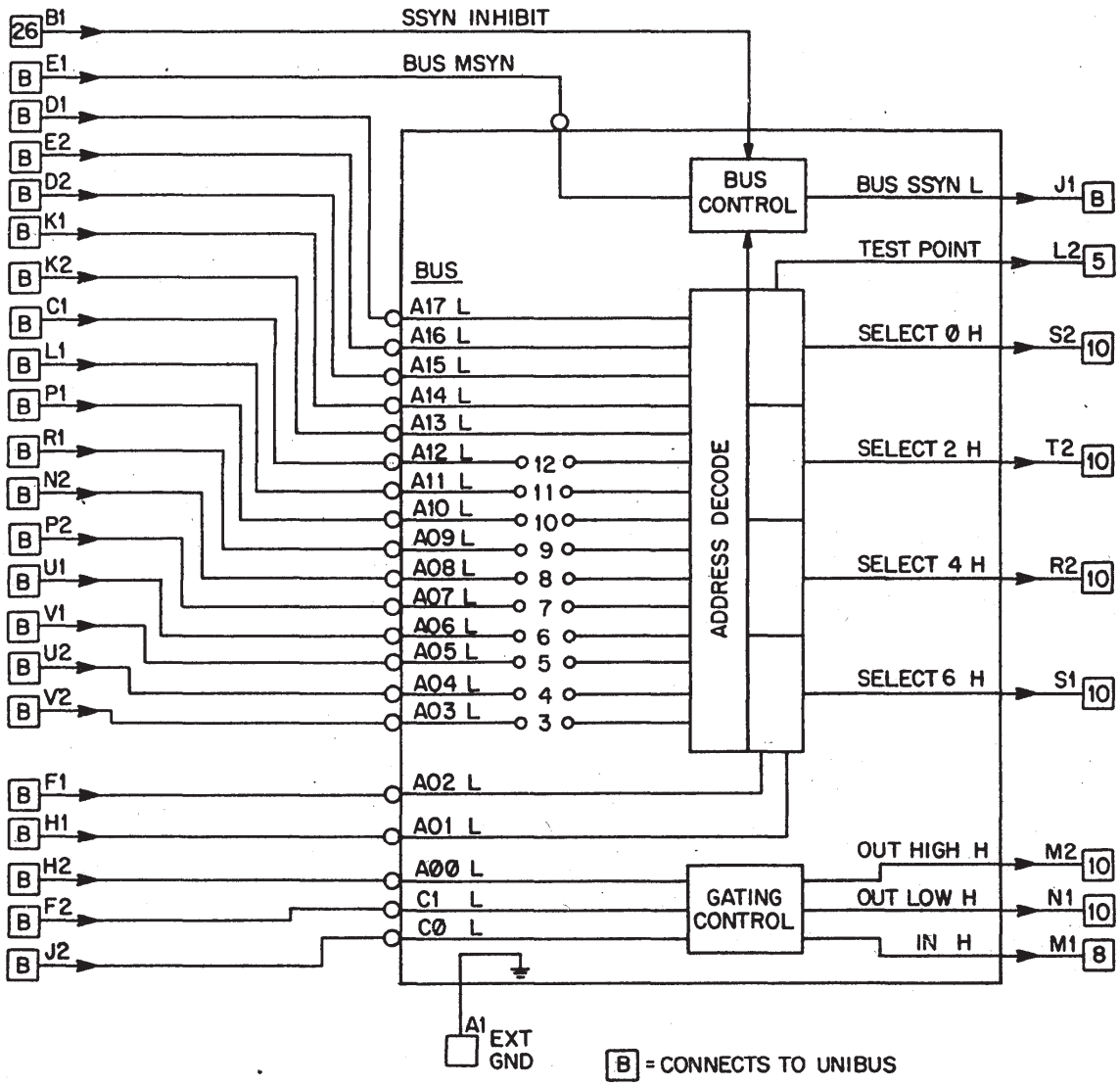
PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$65



Volts	Power mA (max.)	Pins
+5	338	A2
GND		C2, T1

The M105 is used in PDP-11 device interfaces to control the flow of data between the device registers and the UNIBUS. It provides gating signals for up to four device registers that indicate a register is being referenced and three control signals that indicate the path for data flow.

The selector decodes the 18-bit address A <17:00> as follows: A <17:13> defines the memory "page" assigned to peripheral devices (external bank) and must all be asserted. A <12:03> is determined by jumpers on the card.

When the jumper is "in" the selector will look for a zero on that address line. A02 and A01 provide a coding array for the four SELECTED addresses. A00 is for byte control.

Signals for gating control are determined by decoding A00, C1, and C0. The signals obtained are: IN, OUT LOW, and OUT HIGH.

$$IN = DATI + DATIP$$
$$OUT\ LOW = DATO + (DATOB \bullet \overline{A00})$$
$$OUT\ HIGH = DATO + (DATOB \bullet A00)$$

IN is used to gate data from a device register onto the bus. OUT LOW is used to gate D <07:00> into the low byte of a device register. OUT HIGH is used to gate D <15:08> into the high byte of a device register.

In relation to bus control, the M105 is actually the "slave" in the relationship when data transfer occurs on the Unibus.

SSYN is asserted whenever it sees its address being referenced and MSYN is asserted. SSYN is negated when MSYN is negated. There is an approximate 100 nsec. delay between receiving MSYN and the assertion of SSYN to allow for decoding.

EXT GND is used for testing purposes and should be tied to ground in normal operation.

SSYN INHIBIT can be left open when not used.