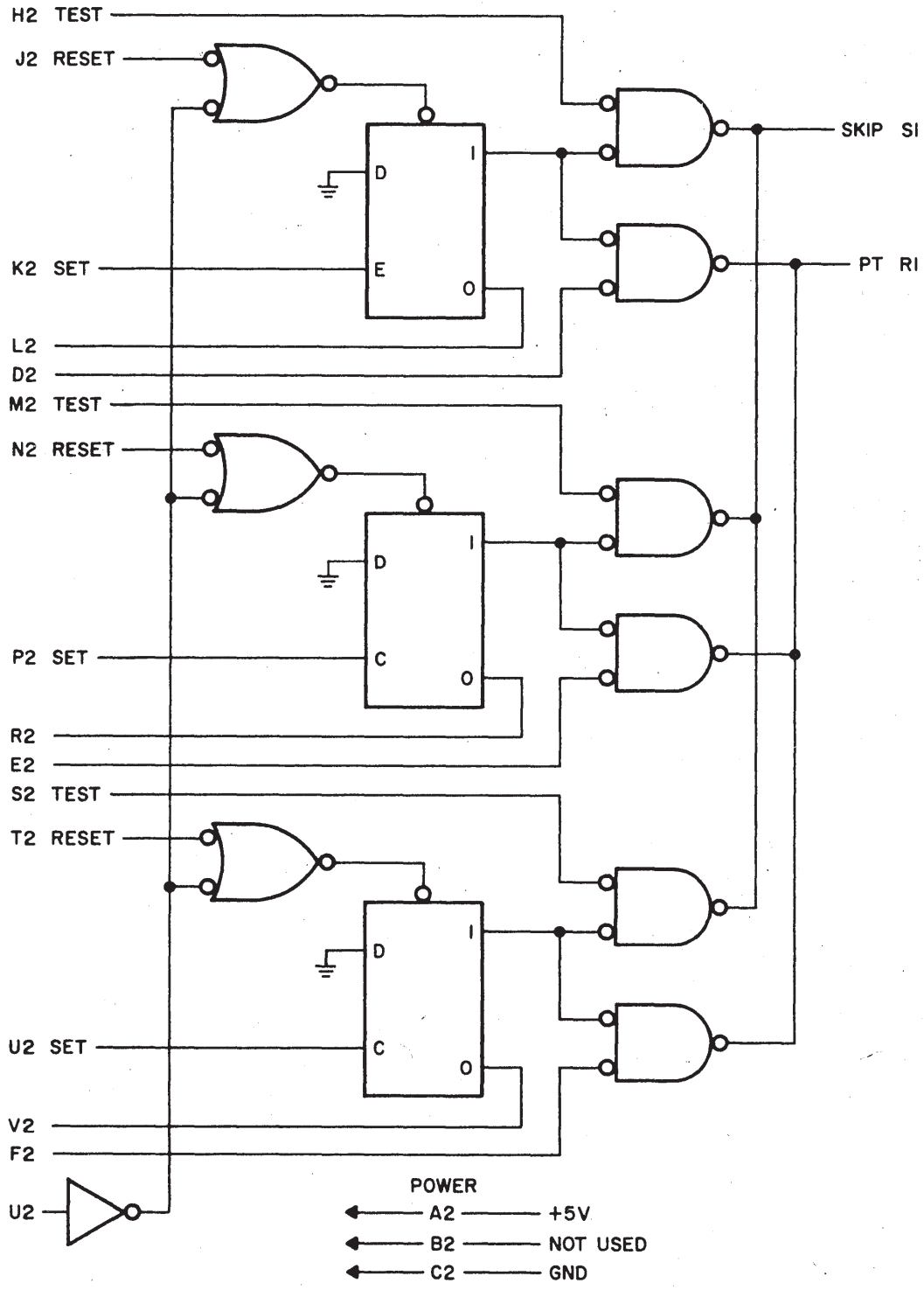
FLAG MODULE
M108

M SERIES



The M108 is a single height module and contains three flag flip-flops. Each flag flip-flop may be independently cleared or all flip-flops may be cleared simultaneously.

The output of each flag flip-flop is gateable and are open collector "OR"ed to the Program Interrupt bus.

The output of each flag flip-flop is passed through a gate and open collector to the skip bus. This facility allows the user to test for a flag.

The "0" side of each flip-flop has been extended to module pins for peripheral control.

Each flip-flop may be independently set by the application of the leading (positive going voltage) edge of a pulse or level to the clock inputs.

If it is not desired to disable the Program Interrupt gate, internal circuitry is provided which makes it unnecessary to connect these inputs to a source of logic "1".

Inputs: K2, P2, U2, present 2 TTL loads. D2, E2, F2 present 1.25 TTL loads. All other inputs present 1 TTL load.

Outputs: L2, R2, V2 supply 9 TTL loads. R1 (P. I. Function) and S1 (Skip Function) are open collector NPN Transistors and will sink 100mA to ground. The voltage applied to these outputs must not exceed +20 volts.

Power: +5 volts at 137 ma. (max.)

M108 — $45