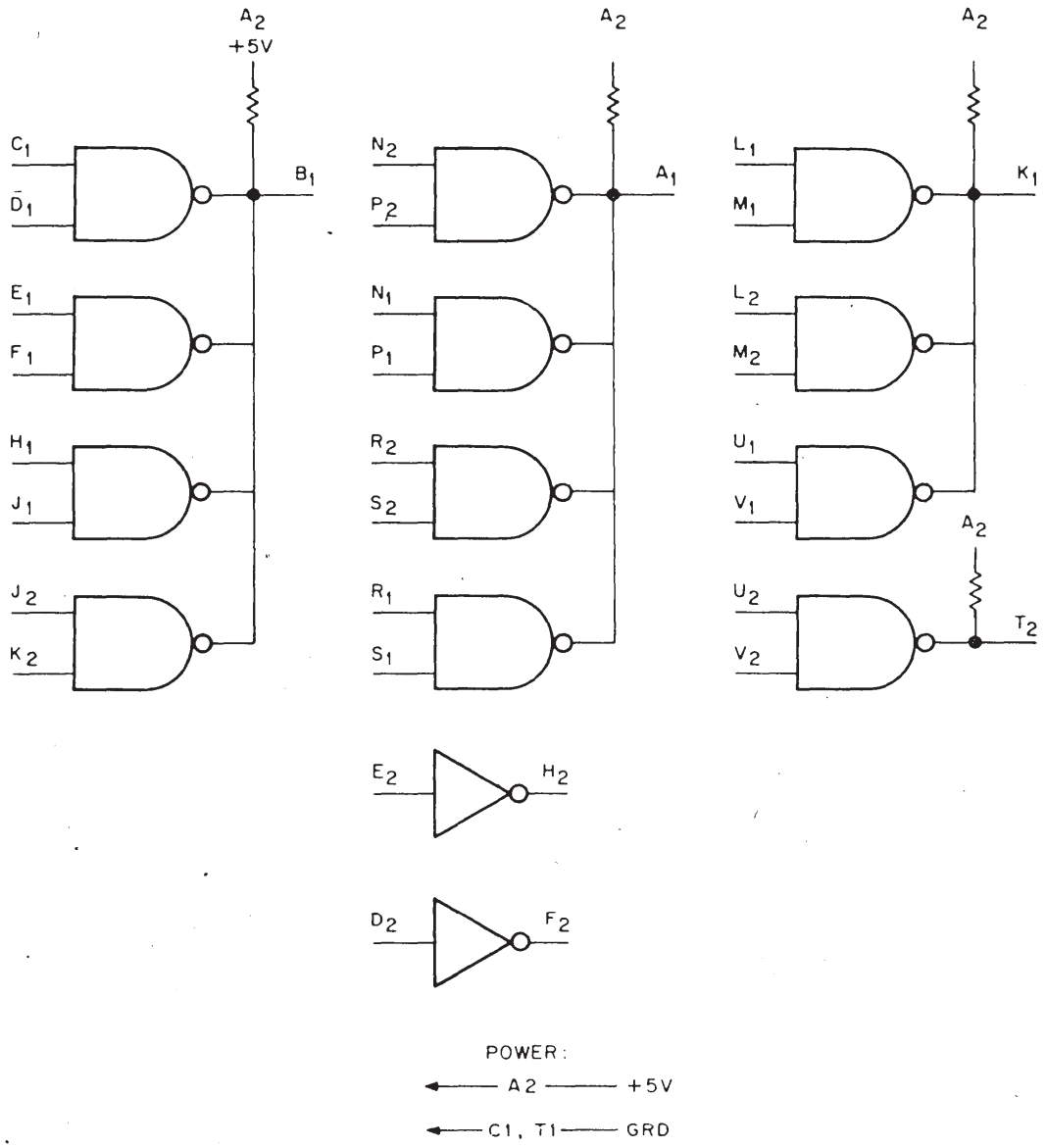
NAND/OR GATES

TYPE M141

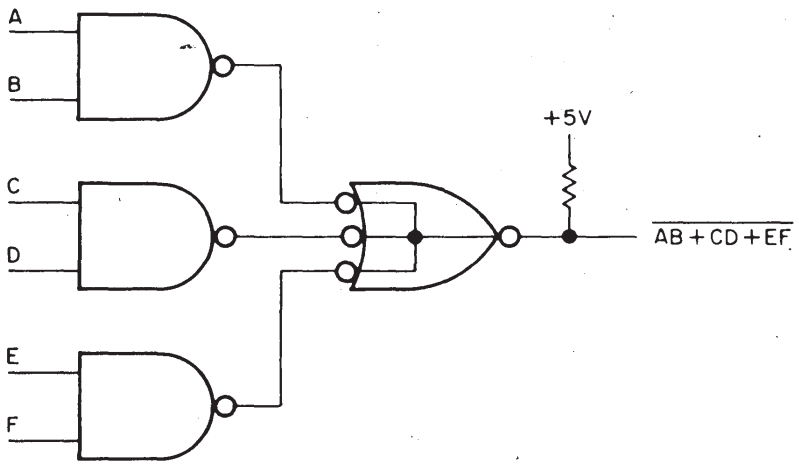
M SERIES



M141 NAND/OR GATE

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor. Propagation delay through these gates is a maximum of 70 nsec.

The NAND/OR gates are arranged in four groups consisting of 4, 4, 3, and 1 two input NAND gates respectively. The outputs in each group are connected together which provide a wired OR for low levels. The function of these gates can be shown as:



By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

Inputs: Each input presents one unit load.

Outputs: Four gate outputs, each capable of driving 7 unit loads. The load resistor of each output presents 2 unit loads when connected to another output. For example, four groups are connected together, therefore 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability. Each inverter output is capable of driving up to 10 unit loads.

Power: +5 volts, 55 ma (avg.)

Propagation delay of the NAND/OR gate with 100 pf capacitance on its output is 70 nsec.

M141—$30.00