M1501
BUS INPUT INTERFACE

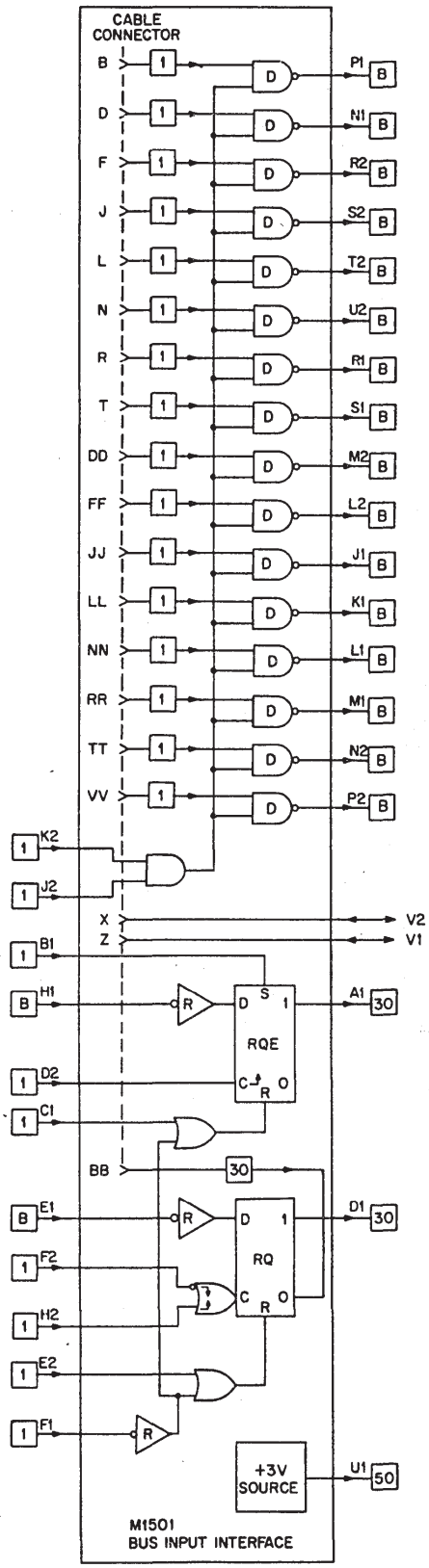
UNIBUS/ OMNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$50



Volts	Power mA (max.)	Pins
+5	300	A2
GND		C2, T1

The M1501 contains 16 bus drivers for interfacing parallel input data to a bidirectional data bus structure such as the PDP-11 UNIBUS or the PDP-8/e OMNIBUS. The module includes two control flags that can be used for interrupt request and enable. Data inputs from an external device enter a 40-pin flat cable connector mounted on the module itself. All inputs are diode-clamped to ground and +5 volts.

APPLICATIONS

This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

Expandability: In PDP-11 applications, up to four M1501 modules (64 bits) can be controlled by one M105 Address Selector module, one M7820 Interrupt Control module, and one M1500 Bus Gates module. Similarly, several M1501's can be combined for multiple word input to a PDP-8/e by using an M1510 Bus Device Selector module.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring.

FUNCTIONS

Input from Cable: Data is gated from the input connector to the bus when both loading inputs (AK2, AJ2) are HIGH.

Send/Receive Control Signal: Two additional lines are provided from the cable connector (Pins X and Z) to the module to allow communications between the device and the computer.

Flags: A request flag (RE) and a request enable flag (RQE) are included on the M1501. Both flags can be cleared on start-up directly from the GENERAL CLEAR bus line. Both flag clock inputs are transition sensitive. The data input to each flag is buffered by a bus receiver; thus, status data can be entered directly from a bus line if desired. The request enable flag clock input responds to a HIGH going transition. The request flag has an input that is sensitive to a LOW going transition and an input that is sensitive to a HIGH going transition. (Whichever input is not used should be connected to the proper logic level to unassert it.) The user is given the maximum degree of freedom to use the request enable flag as a D flop or as an RS flop because all inputs are accessible.

The output of each flag is fully buffered to protect the flag data as well as to provide high output drive.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
40-Pin Connector Inputs	Bus Data Outputs	50
Flag Clock Inputs	Flag Outputs	75