M1502
BUS OUTPUT INTERFACE

UNIBUS/ OMNIBUS

M SERIES

Length:	**Extended**		Power		**Price:**
Height:	**Double**	Volts	mA (max.)	Pins	
Width:	**Single**	+5	750	A2	
		GND		C2, T1	**$100**

The M1502 is a versatile buffered output interface for up to 16 data bits, arranged in two 8-bit bytes. The module accepts data from a bus structure such as that provided in PDP-8/e or PDP-11. Storage flip-flops are included. Outputs are supplied both to a 40-pin flat ribbon connector and to the backplane. Open-collector output drivers with pull-up resistors are included on the module. Three flip-flops with type D as well as type RS inputs are provided as flags or synchronizing devices.

APPLICATIONS

This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

Although intended for parallel data output, this module may be used to drive indicators or relays.

Expandability: In PDP-11 applications, up to four M1502 modules (64 bits) can be controlled by one M105 Address Selector module, one M7820 Interrupt Control module, and one M1500 Bus Gates module. Similarly, several M1502's can be combined for multiple word output from a PDP-8/e, by using an M1510 Bus Device Selector module.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug this module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring.

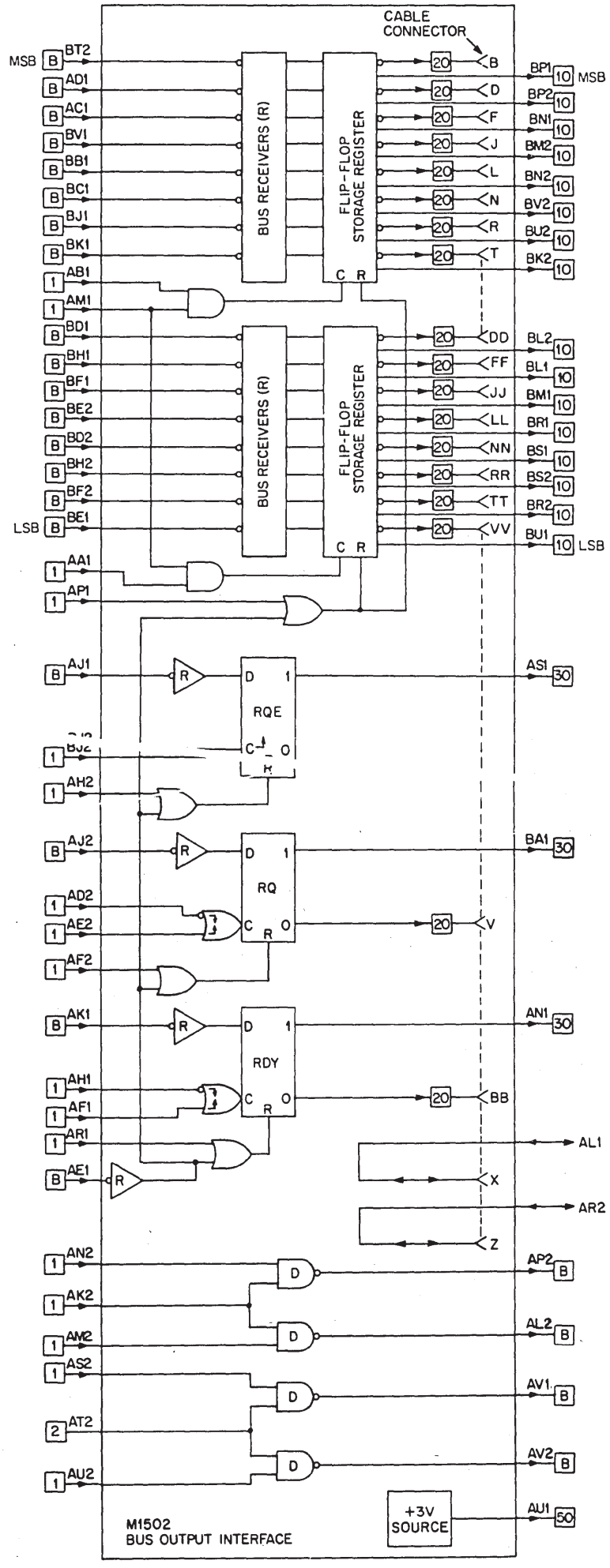
FUNCTIONS

Input from Bus: Data is loaded from the bus to the storage register on a positive transition of the loading input (AM1), which loads all 16 stages. Separate loading inputs are also provided for the lower and upper bytes (AB1 and AA1).

Flags: Three edge-triggered flip-flops are provided. Two of the flags may be triggered by either negative or positive transitions; these supply buffered drive to 40-pin connector outputs. The third flag is triggered by positive-going transitions only, but has a SET input available at the backplane. This flag provides an output to the backplane only.

All flags have separate reset inputs and may also be cleared by a common reset line. The set and reset functions occur on logic HIGH levels. Unused inputs should be connected to a logic level that will unassert them.

Note: Any of the flag outputs can be wired from the backplane to one of the spare bus driver gates (AP2, etc.) for use as READY or INTERRUPT outputs.


CABLE CONNECTOR
BUS RECEIVERS (R)
FLIP-FLOP STORAGE REGISTER
RQE
RQ
RDY
M1502
BUS OUTPUT INTERFACE
+3V SOURCE
MSB
LSB

Spare Lines: Two additional lines are provided between the cable connector and the module for additional communication between the module and the external device. These lines are diode protected against voltage over shoot below —0.75 volts or above +5.75 volts.

SPECIFICATIONS
Propagation Time:

FROM	TO	ns (max.)
BUS DATA Input	40-Pin Output	100
FLAG CLOCK Input	40-Pin Output	150
FLAG SET or CLEAR Input	Backplane Output	100

Output Drive: Outputs to the 40-pin connector are supplied by open-collector high-voltage drivers. Resistors included on the module provide pull-up or current sinking for up to 20 TTL unit loads. If the supplied resistors are removed, the output stages will sink up to 40 mA at logic LOW and will withstand a HIGH level of up to +30 volts. These outputs may therefore be used to drive many types of indicators and even relays. However, if inductive loads are driven, diodes should be wired across each load to swamp inductive kickback.