4.5.5 M163 Dual Binary-to-Decimal Decoder

The M163 consists of two independent binary-to-decimal decoding structures on a single-height module. Each decoder produces a negative true (0V) output for the decimal equivalent of the binary input.

Each decoder can also be used for octal or quad decoding by grounding the MSB, or MSB and the next MSB input lines. Each decoder has a propagation delay of 40 μs (maximum) for input-to-output turnon or turnoff.

Inputs:	Voltage levels of 0V and +3V (typical). All inputs represent 1 TTL unit load each.
Outputs:	Voltage levels of 0V and +3V (typical). All outputs are capable of driving 10 TTL unit loads.
Power:	58 mA (typical) at +5V.

4.5.6 M205 5 "D" Flip-Flops

The M205 module contains five separate D-type flip-flops. Each flip-flop has independent DATA, CLOCK, SET, and CLEAR inputs. Information must be present on the DATA input for 20 ns (maximum) before the CLOCK pulse; the information should remain at the input at least 5 ns (maximum) after the CLOCK pulse has passed the