M1705 **OMNIBUS OUTPUT INTERFACE**

OMNIBUS

M SERIES

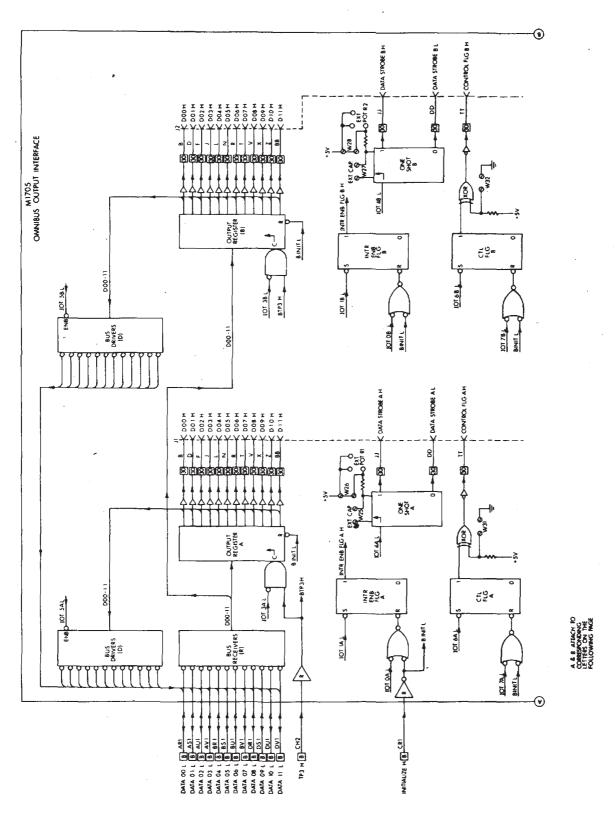
Length: Extended

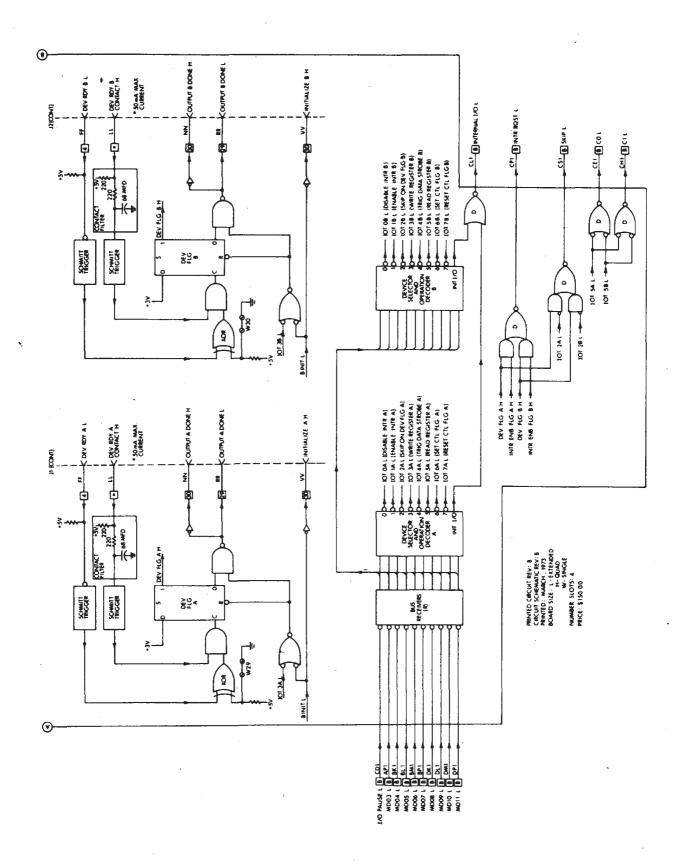
Height: Quad Single Width:

Volts +5 GND

Power mA (max.) 1,15A

Pins AA2, BA2, CA2 All pins F, T, N, AC2, BC1, BC2, CC1, CC2, DC1, DC2





DESCRIPTION

The M1705 is an output interface module that allows the PDP-8 computer to transfer data to, and control the operation of, remotely programmable instruments or similar digital devices. The function is to perform parallel transfers, under program or interrupt control, of 12-bit data words from the computer to peripheral devices.

The M1705 consists of duplicate logic sections. Each section includes device selection logic to address an external device, an operations decoder to determine the type of interface operation, a 12-bit storage register to buffer the output data, interrupt control logic, and bus drivers/receivers to allow operation on the OMNIBUS. Connection to the device(s) is made via standard cables that plug into a pair of connectors on the M1705 module board.

FEATURES

- Complete single-card OMNIBUS output interface
- Data storage registers
- Program interrupt capability
- Cable drivers on all output signals, diode-protected
- Compatible with M1703 OMNIBUS Input Interface
- TTL-compatible signals
- Diode-protection/pulse-shaping on all input signals
- Peripheral I/O cables plug directly onto M1705 card
- Variable pulse width control signals
- User-assigned device codes—jumper selected
- Many user-selected control functions—assertion levels, both TTL and contact closures.

APPLICATIONS

The M1705 OMNIBUS Output Interface is suitable for a variety of scientific and industrial applications which require parallel TTL-compatible data to be output from a PDP-8/E family computer. Its dual word (24-bit) digital output and data storage capability make it a natural for the remote programming of instruments such as digital voltmeters (DVMs), digital multimeters (DMMs), RLC bridges, programmable power supplies and many more.

The M1705 finds application in the scientific and industrial laboratory as a general-purpose digital (TTL) output interface. The control of experimental equipment and the driving of strip chart recorders are only two of the many possible laboratory uses.

Its cable-driving capabilities make the M1705 a fine choice for interprocessor communication. When used with the M1703 OMNIBUS Input Interface, the M1705 provides the capability of communicating at high speed with one or more PDP-8/E family computers. Additionally, the M1703 Input and M1705 Output Interfaces may be combined at one computer to form a general-purpose digital input/output interface system. The result is a very flexible, low-cost system that may be readily expanded. This type of system is often required for the control of, and collection of data from, programmable instruments, production line machinery, lab experiments, and custom peripheral devices (X-Y recorders, card readers, mag tape drivers, etc.).

FUNCTIONS

Device Selection Decoder (A, B)

External devices are addressed through one of two identical Device Selection Decoders. This allows external devices to be handled separately if desired. Each decoder is activated when I/O PAUSE is asserted by the processor and the octal device code for that decoder is received through bits MD03-MD08. Decoders A and B are factory-assigned octal device codes 15 and 16 respectively. However, any octal code from 01 to 77 is selectable by the user via split lug jumpers. The decoder output asserts the INTERNAL I/O line and enables an operation decoder.

Operation Decoder (A, B)

The Operation Decoder decodes the three operation bits MD09-MD11 from the OMNIBUS to determine the type of operation to be performed. The appropriate operation decoder (A or B) is enabled by its respective Device Selection Decoder (A or B).

Output Register (A, B)

The data from the processor accumulator (AC) is transferred to one of the two output registers (A or B) via OMNIBUS lines DATA-00-DATA-11. A binary 1 in the accumulator corresponds to a binary 1 in the output register and to a logic HIGH at the register's output. The register output (D00-D11) may be transferred, in parallel, to the device by a Data Strobe pulse. All bits of both output registers are reset to a logic LOW by assertion of the OMNIBUS signal INITIALIZE.

Device Flag (A, B)

This is a flip-flop which is set by the external device signal DEV RDY or DEV RDY CONTACT and reset by the INITIALIZE signal from the processor or by the appropriate IOT 3 (WRITE REGISTER) command). The status of the Device Flag can be interrogated by the IOT 2 (SKP ON DEV FLG) command. Setting this flip-flop initiates the interrupt request if the Interrupt Enable Flag flip-flop is set.

Interrupt Enable Flag (A, B)

This is a flip-flop which is set under program control to enable or disable the interrupt request function on the M1705 module.

Control Flag (A, B)

This is a spare flip-flop which may be used to perform any additional control function at the external device.

I/O Bus Drivers and Receivers

The OMNIBUS receivers and drivers contain special high-impedance circuitry to minimize bus loading.

PROGRAMMING

The following is a list of instructions that are available for use by the programmer.

Octal Code*	Name	Function
6150	Disable Interrupt A	Resets INTR ENB FLG A to disable the Interrupt Request function for Section A.
6151	Enable Interrupt A	Sets the INTR ENB FLG A to enable the Interrupt Request function for Section A.
6152	Skip on Device Flag A	Asserts the SKIP line if DEV FLG A is set.
6153	Write Register A	Clocks the contents of AC00-AC11 into Output Register A. Also, OUTPUT A DONE H becomes a logic HIGH and OUTPUT A DONE L becomes a logic LOW following completion of this instruction.
6154	Trigger Data Strobe A	The trailing edge of the pulse generated by this IOT initiates DATA STROBE A H and DATA STROBE A L pulses.
6155	Read Register A	Transfers the contents of Output Register A to AC00-AC11.
6156	Set Control Flag A	Sets the CTL FLG A flip-flop.
6157	Reset Control Flag A	Resets the CTL FLG A flip-flop.
6160	Disable Interrupt B	Resets INTR ENB FLG B to disable the Interrupt Request function for Section B.
6161	Enable Interrupt B	Sets the INTR ENB FLG B to enable the Interrupt Request function for Section B.
6162	Skip on Device Flag B	Asserts the SKIP line if DEV FLG B is set.
6163	Write Register B	Clocks the contents of AC00-AC11 into Output Register B.
		Also, OUTPUT B DONE H becomes a logic HIGH and OUTPUT B DONE L becomes a LOW following completion of this instruction.
6164	Trigger Data Strobe B	The trailing edge of the pulse generated by this IOT initiates DATA STROBE B H and DATA STROBE B L pulses.
6165	Read Register B	Transfers the content of Output Register B to AC00-AC11.
6166	Set Control Flag B	Sets the CTL FLG B flip-flop.
6167	Reset Control Flag B	Resets the CTL FLG B flip-Flop.

^{*}Device codes 15_8 and 16_8 are factory-selected. Other codes may be chosen by changing jumpers on the M1705 module.