M191
Carry Look-Ahead Generator

The M191 Carry Look-Ahead Generator, consisting of two DEC 74182 integrated circuits, is a high-speed generator capable of anticipating a carry through a group of ALUs. A 13-ns delay occurs for each look-ahead level.

Input Voltage:	5.5 volts (with respect to network grand terminal).
Supply Voltage:	4.75 − 5.25 (5 v. nominal)
Normalized Fan Out from Each Output:	High logic level 20 Low logic level 10

Each carry look-ahead circuit in the M191 is associated with four ALUs (16 bits). The M191, when used in conjunction with the M159 ALU, provides carry, generate-carry, and propagate-carry functions for 36-bit words. Each circuit generates the anticipated carry through its respective group of ALUs, as well as providing a Generate (G) and Propagate (P) input to a third carry look-ahead circuit associated with the last ALU; hence, the term full-carry look-ahead in three levels (36 bits).

Depending on the selected function of the ALUs, the carry look-ahead circuitry determines whether a carry will be propagated through the particular ALU, or whether the selected function will generate a carry. If a carry is produced, it is directed into the next ALU in line. This sequence is continued for each of the four ALUs in the section. The carry look-ahead circuitry then "looks" at the G and P signals of all four ALUs and determines whether a carry should be inserted into the next four ALUs and into the third level of carry look-ahead. This process is continued for the second section of ALUs (next 16 bits). Finally, the third level of carry look-ahead determines whether a carry should be inserted into the final ALU by examining the resulting G and P inputs of the other two look-ahead circuits.

The truth table for the first-stage carry is as follows:

<div align="center">

True Carry Insert = L

P00	G00	c_{N00}	c_{N+X}
L	L	L	H
L	L	H	H
H	H	H	L
L	H	L	L

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True Carry Insert = Low

P00	G00	C_{N00}	C_{N+X}
L	L	L	H
H	L	L	H
L	H	L	L
H	H	L	L
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	L

The following are the logic equations for a carry look-ahead stage:

$$C_{N01} = C_{N00} * G_0 + G_0 * P_0$$

$$C_{N02} = G_1*P_1 + P_0*G_0*G_1 + G_1*G_0*C_N$$

$$C_{N03} = P_2*G_2 + G_1*G_2*P_1 + G_0 + G_1*G_2*P_0 + G_0*G_1*G_2*C_N$$

$$GG00 = P_3*G_3 + P_2*G_3*G_2 + P_1*G_3*G_2*G_1 + G_3*G_2*G_1*G_0$$
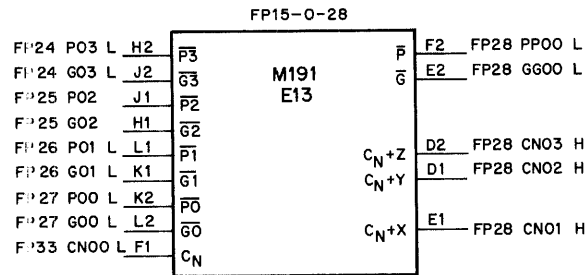
$$PP00 = P_3 + P_2 + P_1 + P_0$$

where

$$C_{NXX} = \text{True L}$$
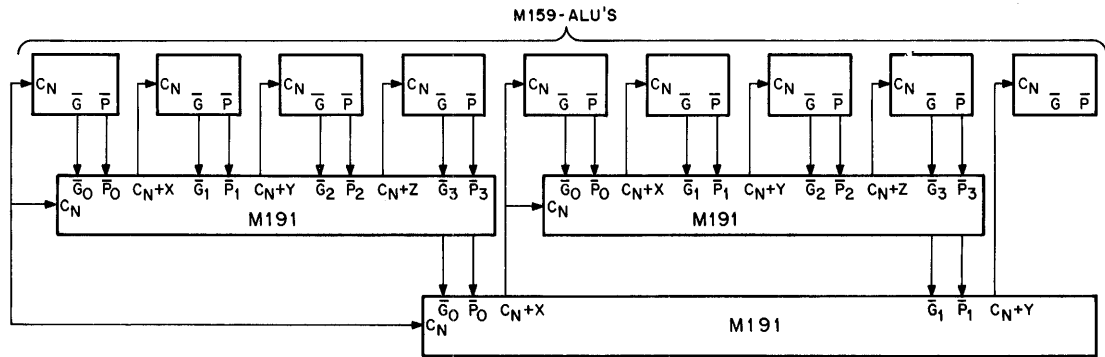
$$GXX = \text{True H}$$

$$PXX = \text{True H}$$

$$GGXX = \text{True H}$$

$$PPXX = \text{True H}$$

FP15-0-28

FP24 PO3 L H2	$\overline{P3}$	M191	$\overline{P}$ F2 FP28 PPOO L
FP24 GO3 L J2	$\overline{G3}$	E13	$\overline{G}$ E2 FP28 GGOO L
FP25 PO2 J1	$\overline{P2}$		
FP25 GO2 H1	$\overline{G2}$		
FP26 PO1 L L1	$\overline{P1}$		C_N+Z D2 FP28 CNO3 H
FP26 GO1 L K1	$\overline{G1}$		C_N+Y D1 FP28 CNO2 H
FP27 POO L K2	$\overline{P0}$		
FP27 GOO L L2	$\overline{G0}$		C_N+X E1 FP28 CNO1 H
FP33 CNOO L F1	C_N		

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36-Bit ALU, Full-Carry Look-Ahead in Three Levels