# M206 General-Purpose Flip-Flops



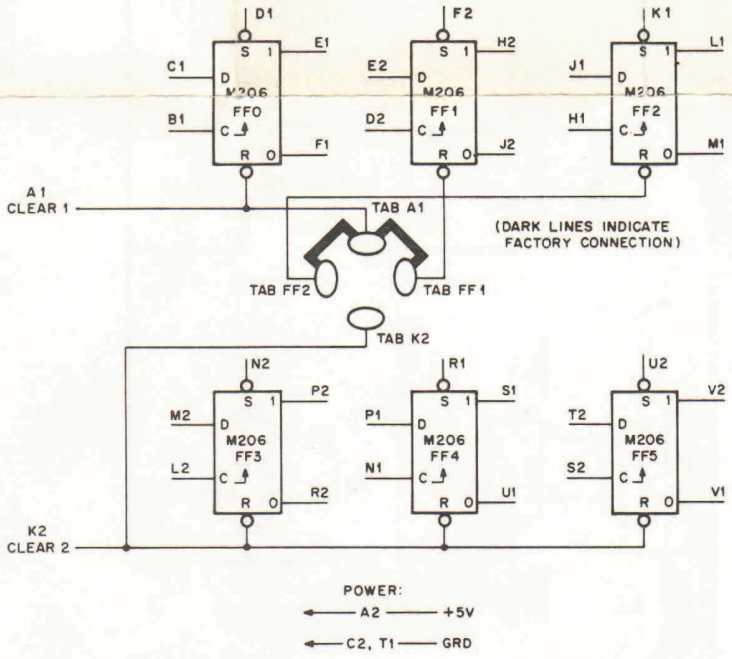
The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

| Configuration | Clear 1 (A1) | Clear 2 (K2) | Delete Jumper | Add Jumper |
|---|---|---|---|---|
| 3-3 | FF0, 1, & 2 | FF3, 4, & 5 | A1 to FF2 | K2 to FF2 |
| 4-2 | FF0 & 1 | FF2, 3, 4, & 5 | A1 to FF2 | K2 to FF2 |
| 5-1 | FF0 | FF1, 2, 3, 4, & 5 | A1 to FF1 | K2 to FF1 |

Information must be present on the D input 20 nsec (max) prior to a standard clock pulse and should remain at the input at least 5 nsec (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 nsec, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

Information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.




**Inputs:** D inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 3 unit loads per connected flip-flop. S inputs present 2 unit loads each.

**Outputs:** Each output is capable of driving 10 unit loads.

**Power:** +5 volts, 87 ma (max).

A common clear for all six flip-flops can be obtained by wiring pins A1 and K2 together externally. **CAUTION:** The loading of each clear line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

Printed Ckt. Rev.: C
Ckt. Schem. Rev.: B