2.13 M216 SIX FLIP-FLOPS

M216 is a single-height module containing six D flip-flops (see Figure 2-25). All flip-flops operate independently except for their clear line, which is shared among three flip-flops.

Data must be present at the D input 20 ns before the clock pulse and should remain 5 ns after the leading edge of the clock pulse has passed the threshold voltage. The flip-flop settles in 50 ns. The CLOCK, DIRECT SET, and CLEAR inputs must be present for at least 30 ns.

Innuta	Valtagas are	standard TTL	lavala
Inputs:	voltages are	Stanuaru IIL	icveis.

Pin	Function	Load
B1,D2,H1,L2,N1,S2	C Inputs	2 units
C1,E2,J1,M2,P1,T2	D Inputs	1 unit
D1,F2,K1,N2,R1,U2	DIRECT SET	2 units
A1,K2	DIRECT CLEAR	9 units

Outputs: Voltages are standard TTL levels. Each output is capable of driving

10 unit loads.

Input/Output Delay: 50 ns

Power Dissipation: 435 mW