0.0 mA when V in = -3V
Propagation Delay 40 ns typ

Outputs: K1 and M1 can drive 10 TTL unit loads. A1, B1, C1, D1, E1, F1 can each drive 37 TTL unit loads. U2 can drive 16 TTL unit loads.

Conversion: Logic Diagram
An active voltage is a True State, i.e., -3V or +3V = "1"
A ground is a True State

Power: +5 V at 130 mA. (maximum).
-15 V at 40 mA. (maximum).

6.4.6 M228 Mark Track Decoder

The M228 mark track decoder is a double-height M-series board designed specifically for the TC08, TC15 DECtape controller. It contains a 9-bit shift register W1-W9, a six-bit state generator, decoding, and control logic. Its operation is explained in detail in Chapter 3 of this manual. The circuit schematic appears in Chapter 7 as Engineering Drawing D-CS-M228-0-1.

Inputs: Standard TTL Voltages	Loading
AV2	26
BH2	18
AS2, BD2, AN2, BR2	1
BC1	12
AR2, BS1, BK2, BL2, BR1	1
AN1	1

Outputs: Standard TTL Voltages	Fan Out
BJ2, BE2, BV2	7
BF2, AK2	8
AL1, AK1, AM2	5
AM1	10
AU1	9
AF1, AH2, BM2, AJ1, AU2, BU1	8
AD2, BT2, BU2	8
AJ2, AT2	6
AF2, BN2, AH1, BP2, BU1, AE2, BS2	10

Power Dissipation: 955 mW at 5V

Application: This module has been designed specifically to perform the mark track decode and state generator functions of the TC08 and TC15 DECtape controller.

6.4.7 W032 Connector

This single-height connector board is intended to be used with 5 cables of 3 conductor shielded coaxial cable. It has no elements. The circuit schematic appears in Chapter 7 as Engineering Drawing B-CS-W032-0-1.

6.4.8 716 Indicator Supply

This power supply delivers 6.5 Vdc and 9 Vac to the indicator panel of the TC08 or TC15 DECtape system. The circuit schematic appears in Chapter 7 as Engineering Drawing B-CS-716-0-1.

Inputs: 115 Vac 50/60 Hz

Outputs: 6.5 Vdc at 4.5A
9 Vac at 100 mA (This is a halfwave rectified signal.)

Power Dissipation: 80W maximum

6.4.9 M623 Bus Driver (see Figure 6-10)

The M623 contains twelve two-input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. Each driver can sink 100 mA at ground and allows a maximum output voltage of +20V. The output consists of an open collector NPN transistor. The circuit schematic appears in Chapter 7 as Engineering Drawing C-CS-M623-0-1.

Inputs: Input levels are standard TTL levels of 0V and +2.4V. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2, and S2 each present one TTL unit load. All other inputs present two unit loads.

Outputs: A driver output will be at ground when both inputs are at ground. Output rise and fall times of TTL are typically 30 ns when a 100 mA resistive load is connected to a driver output. Output voltage must not exceed +20V.

Power: +5V, 71 mA (maximum) plus external load.