M238
Synchronous Up/Down Counter

The M238 Synchronous Up/Down Counter consists of two DEC74193 4-bit synchronous up/down counter integrated circuits. The M238 is used in the EPA, DIR, and DAR registers of the FP15 Floating-Point Processor, where the counters are connected to provide eight bit counting capability.

Synchronous operations is provided by clocking all flip-flops in the counter simultaneously so that the outputs change in coincidence with each other. The flip-flops are master-slave flip-flops and the outputs are triggered by a positive-going transition of either of two clock inputs. One clock input is designated U (up count) and the other is designated D (down count). The direction of counting is determined by pulsing one clock input while the opposite clock input is kept high.

The outputs of the flip-flops may be preset to any state by entering the data at the data inputs while the load input (L) is low. The output will change to reflect the input, regardless of the clock pulses. The clear input is provided to clear all flip-flops, independent of the clock and load inputs.

Both the borrow and carry outputs are available for cascading the up-counting and down-counting operations. When counter underflow occurs, the borrow output produces the same width pulse as the down-count input. When counter overflow occurs, the carry output produces the same width pulse as the up-count input. Cascading is accomplished by applying the borrow and carry inputs to the down-count and up-count inputs of the next counter.

In the example of the DIR register, the UPCOUNT input is inhibited by +3V, indicating that the DIR can only be decremented.