M248
Right Shift Parallel Load Register

The M248 Right Shift Parallel Load Register consists of two DEC7495 Right Shift, Parallel Load Register integrated circuits. The M248 is used in the EPB, FMA, FMB, and FMQ registers in the FP15 Floating-Point Processor. The modules are connected to allow right-shifting between four-bit sections so that each module is capable of handling eight bits. A sample FP15 Floating-Point Processor application is shown in the illustration.

When a logic 0 input is applied to the mode control (MC) input, the output of each flip-flop is applied to the succeeding flip-flop. The right shift operation is performed by clocking at the RS input. During this time, the left-shift (LS) input is inhibited.

When a logic 1 input is applied to the mode control input, the flip-flops are decoupled to prevent right shift and parallel inputs are loaded when the LS input is clocked. The register can be configured for left-shift operations by connecting the output of each flip-flop to the parallel input of the preceding flip-flop.