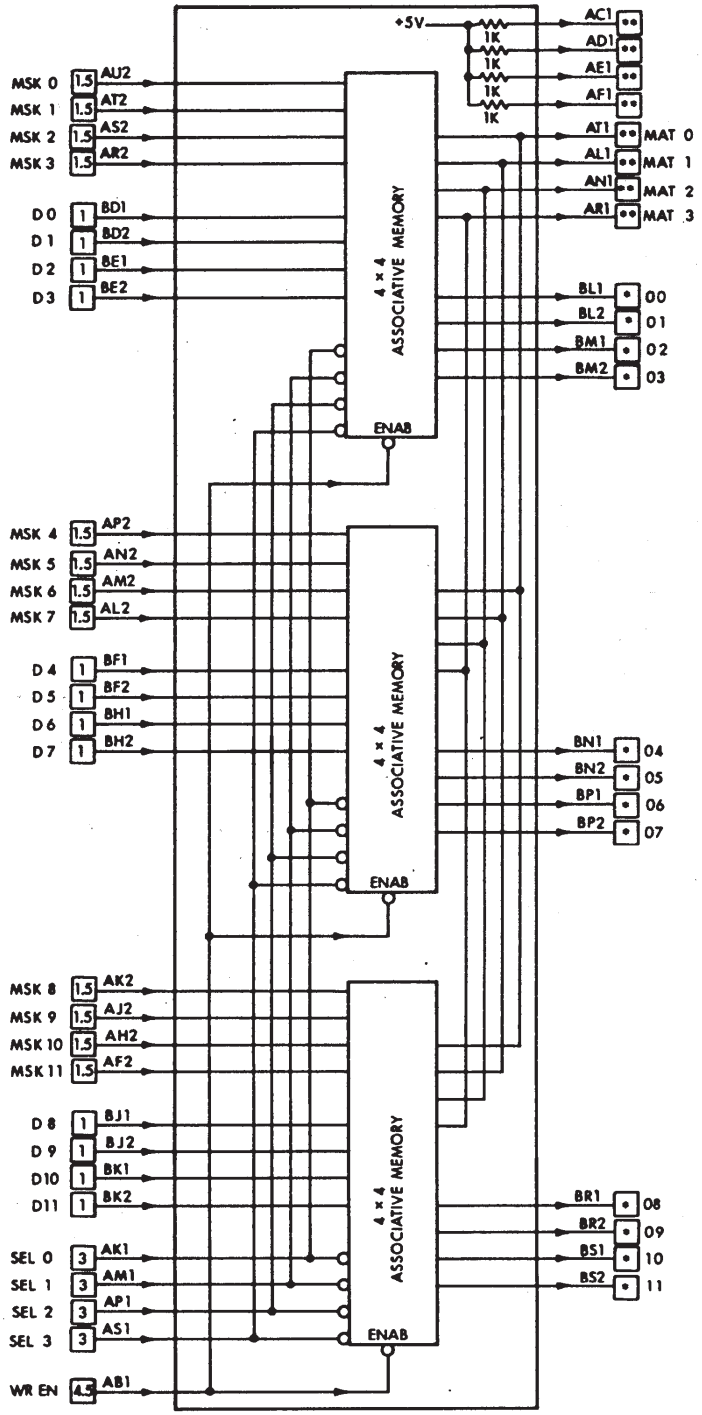
M260
4-WORD X 12-BIT
ASSOCIATIVE MEMORY

FLIP-FLOPS

M SERIES

Length: Standard
Height: Double
Width: Single

Price
$221



*FAN-OUT DEPENDS ON PULL-UP RESISTORS
**REFER TO FORMULA GIVEN IN THE TEXT

Volts	Power mA (max.)	Pins
+5	375	A2

The M260 is a high-speed 48-bit associative random access memory. It is a 4-word by 12-bit array in which the equality search is performed on all bits in parallel. All inputs and outputs are compatible with TTL levels.

To perform an equality search, the 12 bits of data on which the search is to be performed are presented at the data inputs (D0-D11) with the WRITE ENABLE input High and the bit enable lines (MSK0-MSK11) Low. The outputs (MAT0-MAT3) associated with the matched word will then go High.

Because the memory consists of three 4x4 memory units, the match outputs are paralleled as shown in the logic diagram. As an example, for the MAT0 output to go High, bits 0, 4, and 8 of the data word stored in the memory location being addressed would have to equal the corresponding data on input lines D0, D4, and D8. If, however, an MSK input line is held High, a match is forced on the corresponding bit in all words regardless of the state of the data input bit.

Data can be written into the memory through the data inputs (D0-D11) under control of the address inputs (ADD SEL 0 — ADD SEL 3) and the appropriate when the write enable (WR ENB) is Low. When writing information into the memory, both the data and address inputs should reach a stable level at least 10 nanoseconds before the WRITE ENABLE goes Low and both data and address should remain stable for at least 10 nanoseconds after the WRITE ENABLE goes High. Data will be present at the data outputs (00-11) not later than 80 nanoseconds following the High to Low transition of the WRITE ENABLE pulse.

Reading can occur either during an equality search or a write operation. If a single word is addressed, that word will appear at the data outputs. If more than one word is addressed, the wired-OR of the addressed words will appear at the data outputs. Readout is nondestructive.

All outputs are open-collector and require either a pull-up resistor connected to +5 volts, or the M165 module.

The value of the resistor to be used as a pull-up for the outputs should be calculated from the following equation:

Data Outputs:

$$\frac{5.25}{10 - M \cdot L} \leqslant R \leqslant \frac{2.35}{N(.05) + M \cdot H}$$

Match Outputs:

$$\frac{5.25}{10 - M \cdot L} \leqslant R \leqslant \frac{2.35}{N(.55) + M \cdot H}$$

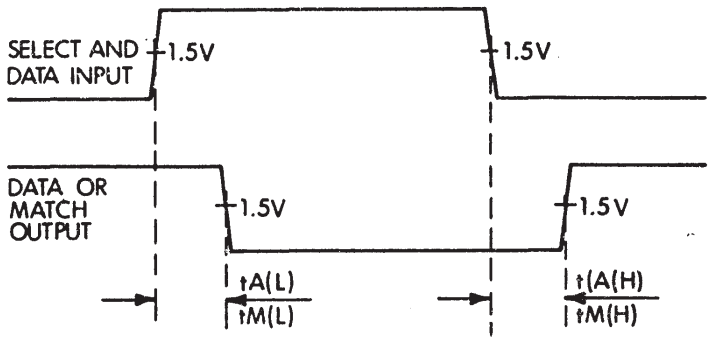
Where: M = number of TTL loads driven by output
N = number of outputs wire-ORed
L = TTL unit load input current at low in mA
H = TTL unit load input current at high in mA
R = pull-up resistor in kilohms

APPLICATION

May be used for comparing and locating data. Can be used as a learning memory, with suitable gating, by loading any word into memory which is not already contained in storage.

SPECIFICATIONS

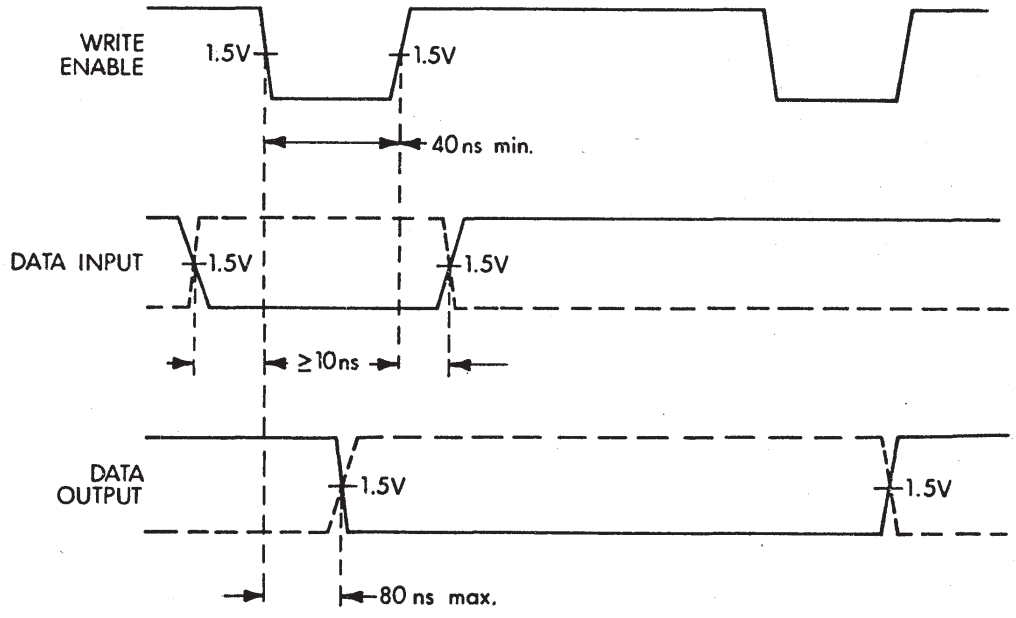
Propagation Delay:



Address to data output delay	t_A (L)	=	30 ns	maximum	0 ns	minimum
	t_A (H)	=	35 ns	maximum	0 ns	minimum
Data bit to match output	t_M (L)	=	35 ns	maximum	0 ns	minimum
	t_M (H)	=	40 ns	maximum	0 ns	minimum

Maximum Capacitive Load: 30 pF for access and matched delays to be within their specified maximum values.

Timing:



This diagram assumes that the address line is Low at least 10 nanoseconds before the WRITE ENABLE goes Low and remains Low for the remainder of the diagram.