M261
FOUR-STATE MOTOR TRANSLATOR

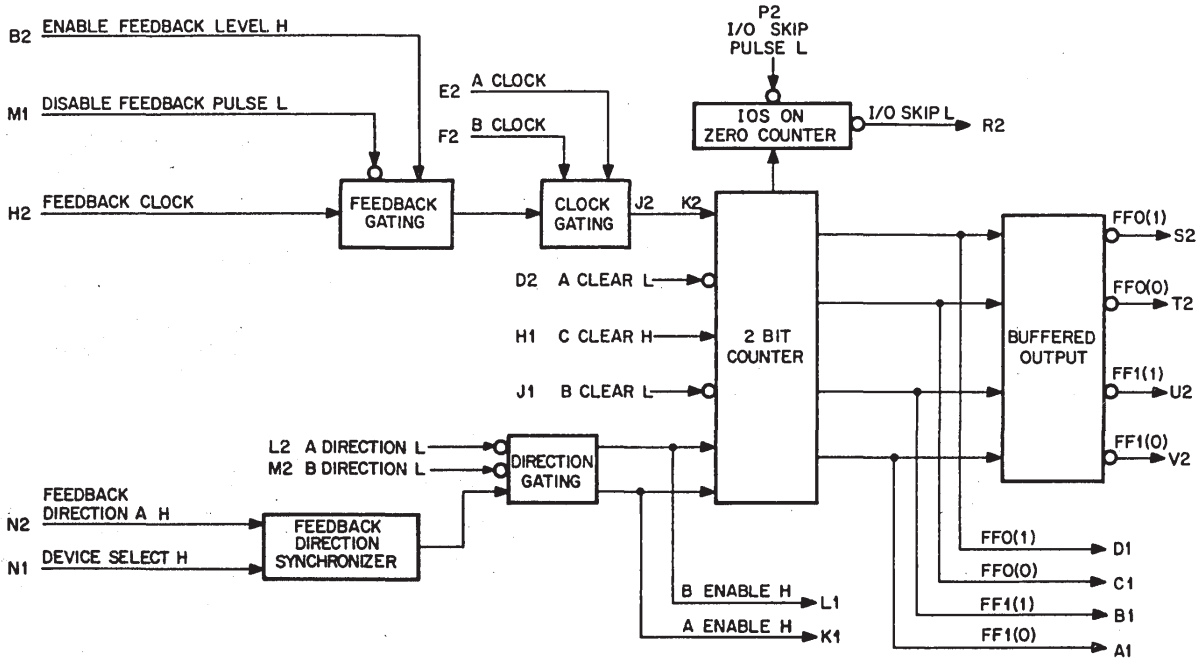
MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$40



Volts	Power mA (max.)	Pins
+5	175	A2
GND		C2, T1

The M261 motor translator will develop the sequence of patterns necessary to step a Sigma or Superior Electric type stepping motor (4 winding). It is a 2-bit switch-tail ring counter which, if initially cleared, would be in state 1. (Fig. 1)

State	Flip Flop	0	1
1		0	0
2		0	1
3		1	1
4		1	0

FIGURE 1

State	Winding	A	B	C	D
1		1	1	0	0
2		0	1	1	0
3		0	0	1	1
4		1	0	0	1

1 = current supplied to winding

FIGURE 2

The state sequence (1, 2, 3, 4, 1, . . . or 1, 4, 3, 2, 1, . . .) is determined by the direction gating. The pattern for motor stepping (Fig. 2) is achieved by assigning flip flop outputs to windings; A-FF1(1), B-FF0(1), C-FF1(0), D-FF0(0). These buffered flip flop outputs can enable K-series DC drivers to energize the selected winding.

The translator is clocked by a High to Low transition on A CLOCK or B CLOCK. The ORed clock signal must be jumpered externally to the counter (J2-K2). DIRECTION is stored in an RS flip flop and can be loaded by asserting one of the direction inputs Low. This arrangement facilitates the use of M103 or M107 device selectors; the first pulse of an IOT (input/output transfer instruction) sets the direction, the second clocks the counter.

For closed loop operation, the direction flip flop may be synchronized with the motor shaft rotation. If there is a direction level available from the transducer, this level should be asserted high when the direction of rotation is the same as that represented by the A DIRECTION L input to the flip flop. This gating may be disabled by DEVICE SELECT H. The clock input for feedback operation is a Low to High transition and is ORed with the other clocks after gating. The two gating signals are an enable, asserted High, and a pulse or level asserted Low which truncates the clock pulse after it has made its transition. This is necessary because the clock signal is from an asynchronous device and is often a square wave which remains High a long time (20-100 μs) after the clocking transition. This High level at the clock input of the counter will mask subsequent transitions on the other clock inputs.

This module may be used in conjunction with the I/O skip facility on a computer. An IOT at I/O SKIP PULSE L and both flip flops in the zero state will cause I/O SKIP L to be generated.

The unbuffered flip flop outputs are available for additional gating. These lines are electrically distinct from the buffered outputs.