

M262 TEN-STATE MOTOR TRANSLATOR

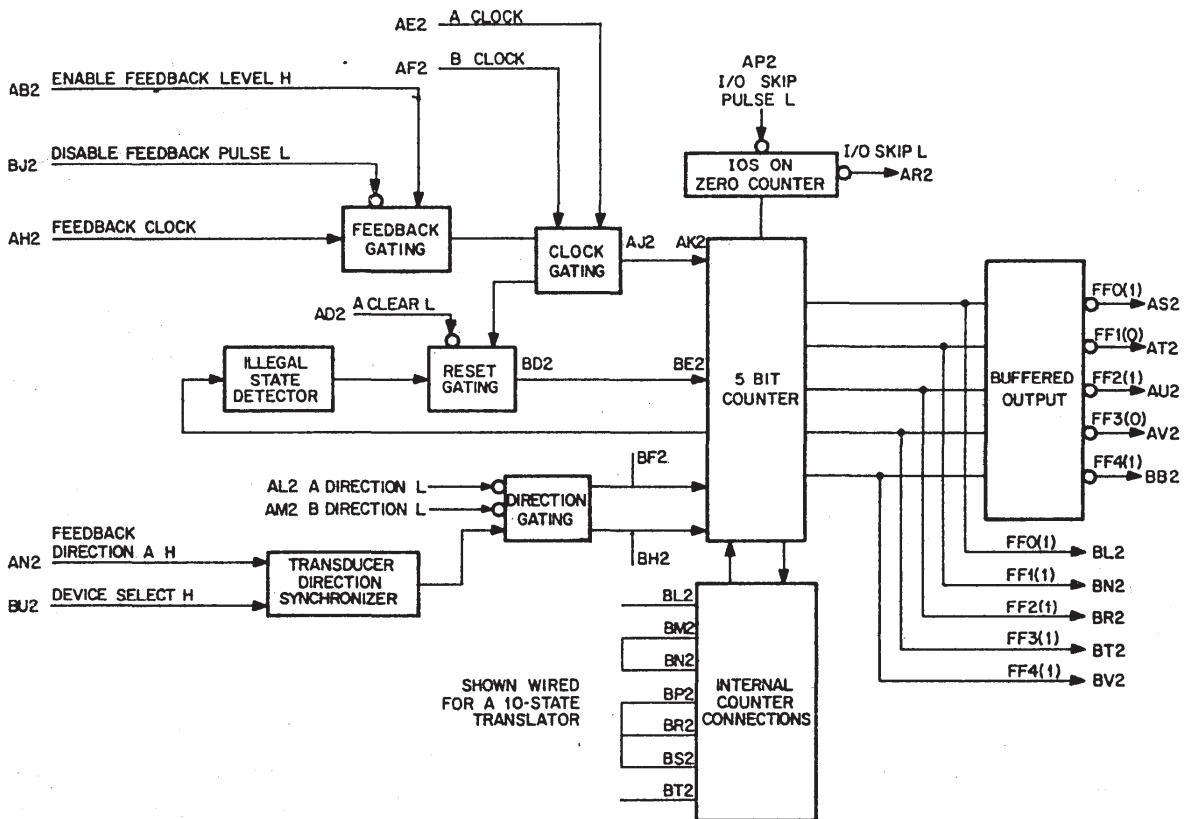
MISCELLANEOUS

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

\$65



Volts +5 GND	Power mA (max.) 350	Pins AA2, BA2 AC2, BC2
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The M262 motor translator will generate the sequence of patterns necessary to step a Fujitsu type stepping motor (5 winding). It is a double height module with a five bit switch-tail ring counter which may be truncated to four or three bits by external jumpers.

BM-BN
BP-BR
BR-BS

BM-BN
BP-BN
BT-BS

BL-BP
BT-BM

10-state jumpers

8-state jumpers

6-state jumpers

State	FLIP	FLOP	0	1	2	3	4
1			0	0	0	0	0
2			1	0	0	0	0
3			1	1	0	0	0
4			1	1	1	0	0
5			1	1	1	1	0
6			1	1	1	1	1
7			0	1	1	1	1
8			0	0	1	1	1
9			0	0	0	1	1
10			0	0	0	0	1

FIGURE 2

State	Winding	A	B	C	D	E
1		1	1	1	0	0
2		0	1	1	0	0
3		0	1	1	1	0
4		0	0	1	1	0
5		0	0	1	1	1
6		0	0	0	1	1
7		1	0	0	1	1
8		1	0	0	0	1
9		1	1	0	0	1
10		1	1	0	0	0

FIGURE 3

1 = current supplied to winding

FF2 is removed for the 8-state counter and both FF1 and FF2 are bypassed for the 6-state counter.

After the counter is cleared it will be in state 1. (Fig. 2) The state sequence (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 1 . . . or 1, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1 . . .) is determined by the direction gating. The pattern for motor stepping (Fig. 3) is achieved by assigning flip flop outputs to windings; FF0(1)-A, FF2(1)-B, FF4(1)-C, FF1(0)-D, FF3(0)-E. These buffered flip flop outputs can enable K-series DC drivers to energize the selected windings.

The translator is clocked by a High to Low transition on A CLOCK or B CLOCK. The ORed clock signal must be jumpered externally to the counter (AJ-AK). Direction is stored in an RS flip flop and can be loaded by asserting one of the direction inputs Low. This arrangement facilitates the use of M103 or M107 device selectors; the first pulse of an IOT (input output transfer instruction) set the direction, the second clocks the counter.

With a 5-bit counter there are 32 (2^5) possible states, but the counter is clocked through a ring of only 10 states (Fig. 2). Gating is available to detect illegal states and clear the counter to state 1. This gating must be connected by an external jumper (BD-BE).

For closed loop operation, the direction flip flop may be synchronized with the motor shaft rotation. If there is a direction level available from the transducer, this level should be asserted High when the direction of rotation is the same as that represented by the A DIRECTION L input to the flip flop. This gating may be disabled by DEVICE SELECT H. The clock input for feedback operation is a Low to High transition and is ORed with the other clocks after gating. The two gating signals are an enable, asserted High, and a pulse or level asserted Low which truncates the clock pulse after it has made its transition. This is necessary because the clock signal is from an asynchronous device and is often a square wave which remains high a long time (20-100 μ s) after the clocking transition. This High level at the clock input of the counter will mask subsequent transitions on the other clock inputs.

This module may be used in conjunction with I/O skip facility on a computer. An IOT at I/O SKIP PULSE L and both flip flops in the zero state will cause I/O SKIP L to be generated.

The unbuffered flip flop outputs are available for additional gating. These lines are electrically distinct from the buffered outputs.