For use as a delay the M304 is useful as a 1-μs one-shot delay without connecting B1, etc. Delay accuracy is ±10 percent and is not adjustable. Propagation delay to the leading edge of the low output should be less than 80 ns.

Inputs: Two inputs to each delay function as low OR inputs. One unit load must be provided for each gate. Input signals are differentiated and require that the rate of fall of input signals be greater than 2V/μs.

4.5.12 M307 Integrating One-Shot

The M307 consists of two retriggerable one-shot delays, potentiometers, and capacitors on a single-width double-sided module. Provision is made for selection of one six delay ranging from 0.5 μs to 0.5s by module pin connections. Potentiometers are provided on the module for continuous variation of delay time over a 10-to-1 range.

Inputs:

Low OR inputs: Pins K2 and L2 (U1, S1) constitute a logical low OR input. Delay time commences at the transition of either of these pins from +2V to +0.45V. Loading at each input is 60 μA to +4.2V, 1.6 mA to ground.

When using the inputs K2 and L2 (U1, S1) to trigger the delay, all other inputs must be more positive than 2.4V.

High input: Pin J2 (N1) triggers the delay on the positive transition of the input signal. Loading at this input is the same as above.

When using pin J2 (N1) to trigger the delay, one or both of the low OR inputs must be less than +0.2V and pin L1 (M1) must be more positive than +2.8V.

dc input: A low input to pin L1 (M1) causes the output of the delay to become asserted and remain asserted for a time equal to the time pin L1 (M1) remains at ground plus the time of the delay.

Output: All outputs have a 10 unit load driving capability.

Delay Range:	Pin Connections Circuit 1	Pin Connections Circuit 2
0.5 μs to 5 μs	None	None
5 μs to 50 μs	D1 to D2	U2 to M2
50 μs to 500 μs	B1 to D2	V2 to M2
500 μs to 5 ms	E1 to D2	S2 to M2
5 ms to 50 ms	F1 to D2	R2 to M2
50 ms to 0.5s	H1 to D2	P2 to M2

External capacitors may be connected from pin J1 to D2 (N2 to M1). Electrolytic capacitors must be polarized positive (+) to pin J1 (N2). Wiring to these pins must be extremely short. It is recommended that external capacitors be connected to a W994 blank module and located adjacent to the M307.

Potentiometers are provided on the module for continuous variations of delay time over a 10-to-1 range. To connect the internal potentiometers, connect pin A1 to C1 (V1 to P1). External fine adjustment of the delay time may be accomplished by a Vernier consisting of a 100K rheostat connected from +5V to pin C1 (P1).

Power Requirements:			
	Pin A2	+5V	70 mA
	Pin B2	-15V	0 mA
	Pin C2, T1		GND

4.5.13 M611 Power Inverter Module

The M611 is a single-height module that contains 14 DEC 74H70 high-speed power inverters. The M611 is used in the RK11 for signal inversion to provide high drive compatability of internal signals, for example, the generation of the CLR MSR signal (see Paragraph 3.4.1).

Inputs: Pins A1, D1, F1, E2, J1, H2, L1, K2, N1, R1, P2, V1, S2, and U2 are inputs of the M239 that input 1 TTL fast-series unit load.

Outputs: The output pins of the M239 are B1, E1, H1, K1, J2, M1, L2, P1, S1, R2, U1, T2, and V2. Each output can drive up to 80 TTL unit loads of fast-series gates with D2 as the +3V reference. The worst-case delay is 20 ns, with 30 TTL unit loads. Minimum delay is 10 ns.

4.5.14 M797 Register Selection Module

The M797 is a single-height module used to decode one of eight possible register addresses in conjunction with the M105 module (see Table 4-1 for M105 reference). In addition, control signals are used to select a Read, Write low byte, or Write high byte.

4.5.14.1 Theory of Operation – The M797 contains three BCD/DEC decoders of which outputs 0 through 7 are used to select a register. Outputs 8 and 9 are used to create a gating strobe. The module is enabled by the input at V1 (DEV SELD) at which time the control signals at A1 and D1 select the correct decoder(s) for the operation specified. Once a decoder or decoders has been selected, its 8 and 9 outputs are driven high, asserting STRT XTIM output at H1. One of the 0 through 7 outputs of the decoders is selected by the inputs at B2, B1, and C1. These inputs are inverted before reaching the decoders so that if they are all high the 0 output of the decoder will be selected. The input at V2 can be used to prevent the selection of the two decoders used to write into a register when it is asserted H (i.e., BUSY H). The exception to this is when the three address inputs are high (i.e., selection of a control register). In the RK11, this feature is not used and V2 is grounded.

4.5.15 H734 Power Supply

The H734 Power Supply supplies the dc for the disk drives of the RK11 System. Each H734 supplies power to two drives. The H734 has overvoltage protection with the crowbar at ±16.5 Vdc. The H734 also contains an undervoltage detection of ±13.7 Vdc and low input voltage detection at approximately 100V. Both positive and negative voltages in the H734 are regulated by two switching mode voltage regulators. These two circuits operate from a rectified filtered dc voltage of ±25V ±2V ripple. The regulators contain differential amplifiers that compare the regulator output to a stable reference and adjust the output accordingly to either increase or decrease its level.

Input Voltage: H734A 115V ± 10% 6A
H734B 230V ± 10% 3A

Output Voltage: +15 Vdc ± 5% at 12A
-15 Vdc ± 5% at 12A