2.15 M149 9 X 2 NAND "WIRED OR" MATRIX

The M149 is a single-height module containing two sets of 9-open collector NAND gates wired together in an OR function to form nine output pins. The M149 also includes a pulse amplifier (see Figure 2-28).

Inputs:	Voltages are standard TTL levels. Input loading is 1 unit per input.
Outputs:	Voltages are standard TTL levels. Each output except V1 is an open collector that can sink 16 mA. The output at V1 can drive 10 unit loads.
Input/Output Delay:	10 ns at output
Power Dissipation:	350 mW
Application:	This module is generally used to gate signals onto an open collector bus.

2.16 M500 NEGATIVE RECEIVER MODULE

M500 is an M-series single-height module containing eight I/O bus receivers that can accept negative logic levels and convert them to positive levels (see Figures 2-29, 2-30, and 2-31). Each M500 receiver has a negative input clamped to 0V and -3V. The threshold switching level is -1.5V with an input current of 100 μA.

Inputs:	Minimum input impedance at 0V: 30 kΩ Maximum current load to bus: 100 μA Inputs are standard negative logic levels of 0 and -3V.
Outputs:	Fan Out Output No. 1: 12 units Output No. 2: 11 units Input/Output No. 1 delay: 50 ns Input/Output No. 2 delay: 40 ns Outputs are standard TTL logic levels.
Power Dissipation:	750 mW max from -15V 800 mW max from +5V
Application:	The M500 module was designed to receive PDP-9 I/O bus signals for devices using positive logic. It provides a high input impedance.

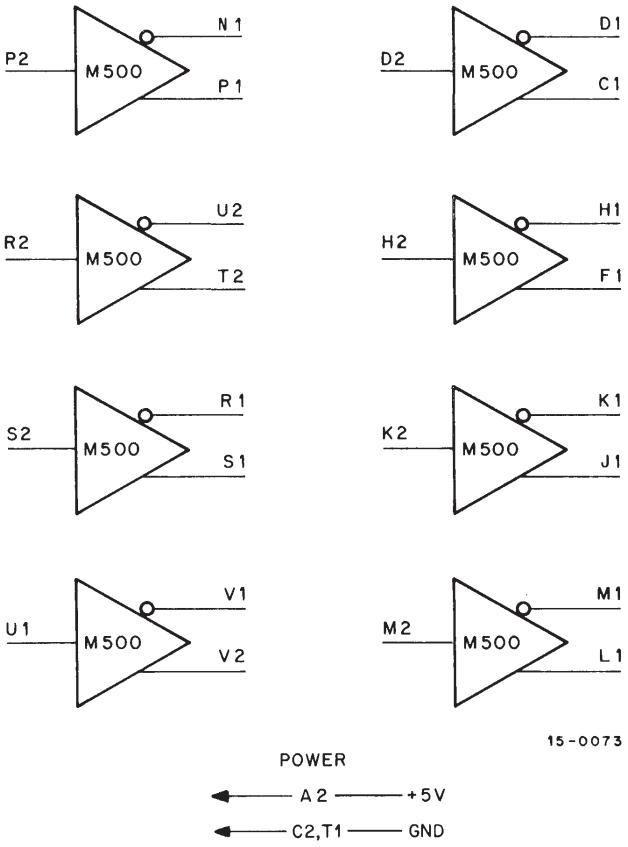

Figure 2-29 M500 Negative Receiver, Block Schematic