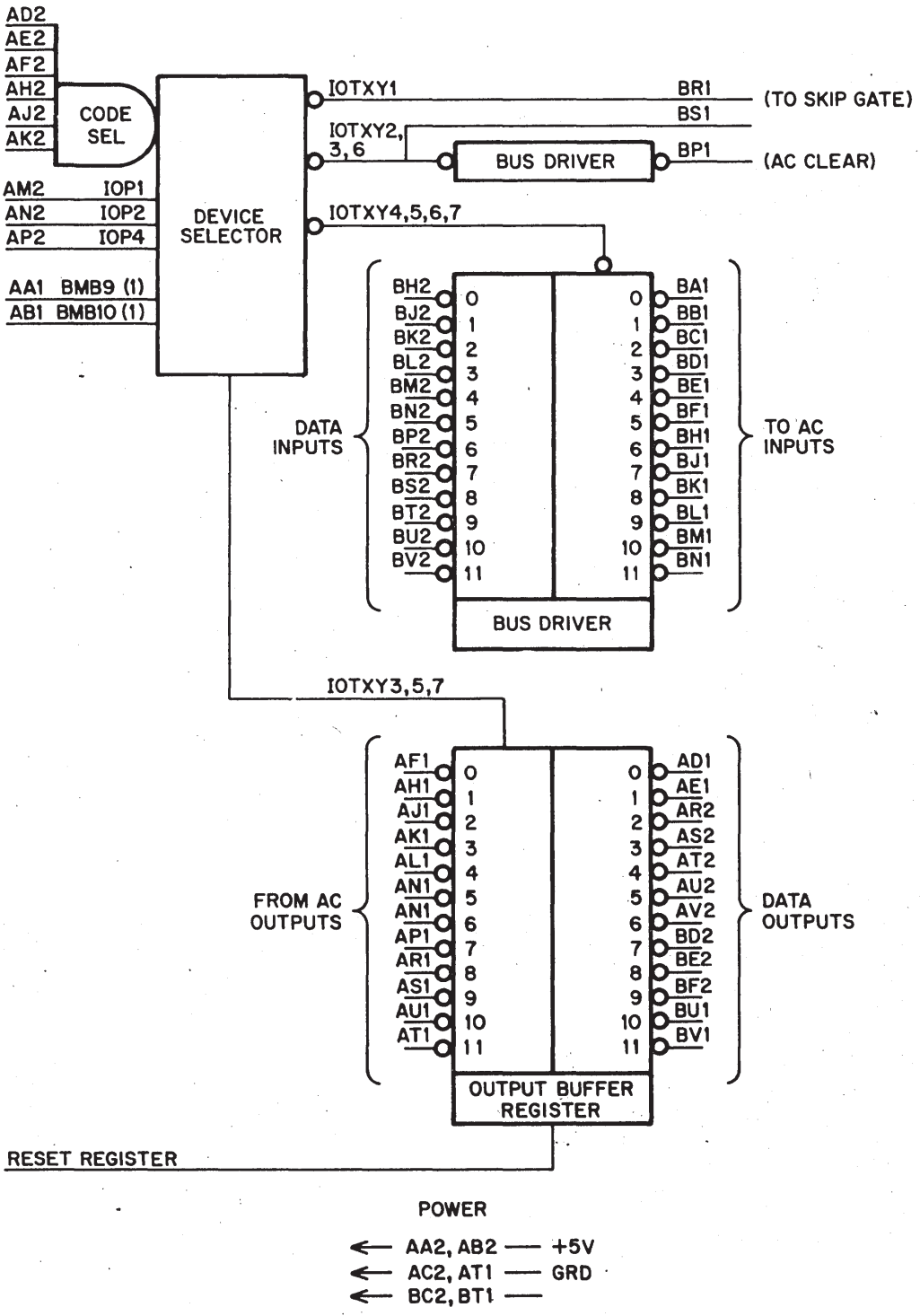
I/O BUS TRANSFER REGISTER
M735

M SERIES



The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

Inputs:
All inputs present one TTL unit load with few exceptions as noted in the functional descriptions below:

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse input gates for IOP1, IOP2, and IOP4 are enabled for use as detailed below. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts. These inputs are all clamped so that no input can go more negative than —0.9 volts. When this module is used with the PDP8/I or PDP8/L these inputs would be connected to BMB outputs 3-8 to generate a device code. Where required in discussions below, this 6-bit device code will be referred to as code XY.

I0P1, 2, 4, BMB9(1) and BMB10(1): These three IOP's 50 nsec or longer positive pulse inputs, in conjunction with control level inputs BMB9(1) (Pin AA) and BMB10(1) (Pin AB1) provide all of the necessary signals for operation of this module. Table 1 below indicates the recommended use of these pulses and levels. A"1" or "0" in this table indicates the presence or absence respectively of a pulse (an IOP) or the logic level at pins AA1 or AB1.

The M735 module operation as associated with the various mnemonic IOT codes is quite explicit with the exception of IOTXY5. This code (IOTXY5) would be used to load zeros into the M735 with IOTXY1 and then to load into the AC the data present at the data inputs of the bus driver when IOTXY4 occurs. In this particular operation the AC has been effectively cleared as the content of the AC was zero during IOTXY1 thereby allowing the transfer of data into the AC without the use of the AC clear command usually generated by IOT2.

IOP 4	IOP 2	IOP 1	BMB 9(1)	BMB 10(1)	PDP/8 Mnemonic	Module Operation
0	0	1	0	0	IOTXY1	+3V → OV output pulse on pin BR1 used for skip function.
0	1	0	0	1	IOTXY2	+3V → OV output pulse on pin BS1, bus driver output on BP1 pulsed to ground and is used for the AC clear function.
0	1	1	0	1	IOTXY3	Load output register from accumulator outputs on IOP1 execute IOTXY2.
1	0	0	1	0	IOTXY4	Data inputs strobed onto accumulator inputs.
1	0	1	1	0	IOTXY5	Load output register on IOP1, Execute IOTXY4.
1	1	0	1	1	IOTXY6	Execute IOTXY2, and IOTXY4.
1	1	1	1	1	IOTXY7	Execute IOTXY3, and IOTXY4.

Although it is not implicit from Table 1, BMB9(1) and BMB10(1) inputs are gated in a positive OR circuit, so that when the M735 is not used on a PDP8/I or PDP8/L I/O bus one of these inputs can be grounded and the other used for control. They must appear at least 50 nsec prior to an IOP pulse. If the M735 is used with one of the above computers, these inputs must be tied to the corresponding I/O bus lines. The input load on IOP1 is two TTL unit loads. All five inputs are clamped so that no input can go more negative than —0.9 volts.

Data Inputs: Each data input when at ground, enables the corresponding bus driver output to be pulsed to ground during IOTXY4. A high input will inhibit the bus driver from being strobed. Since each input is ANDed with IOTXY4, any change of data after this strobe begins will change the bus driver output.

Accumulator Inputs: The input level presented to these inputs will be the same as that assumed by the buffer outputs after executing inputs strobes IOTXY , 5, or 7. Input data must be present at least 50 nsec prior to an IOP. Each input is protected from negative undershoot by a diode clamp.

Reset Register Pin AL2: A positive pulse of 50 nsec or longer at this input sets all buffer outputs to ground. When high, this input overrides any data loading from the accumulator inputs. The output register will be cleared within 70 nsec from the rising edge of this input. Diode input clamping is provided to limit negative undershoot to —0.9 volts.

Outputs:
Pin BR1: This output can drive ten TTL unit loads and has a propogation delay of less than 20 nsec. See Table 1.

Bus Driver: These open collector npn transistor bus driver outputs, including pin BP1, can sink 30 ma. at ground. The maximum output voltage cannot exceed +20 volts and each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L,

output pins BA1—BN1 would be connected to the accumulator input lines and pin BP1 to the clear accumulator line of the I/O bus. Typical rise and fall TTT of these outputs with a 30ma resistive load are 100 nsec.

Buffer Outputs: Each output can drive ten TTL unit loads.

Power: +5 volts at 385 ma. (max.)

M735 — $140