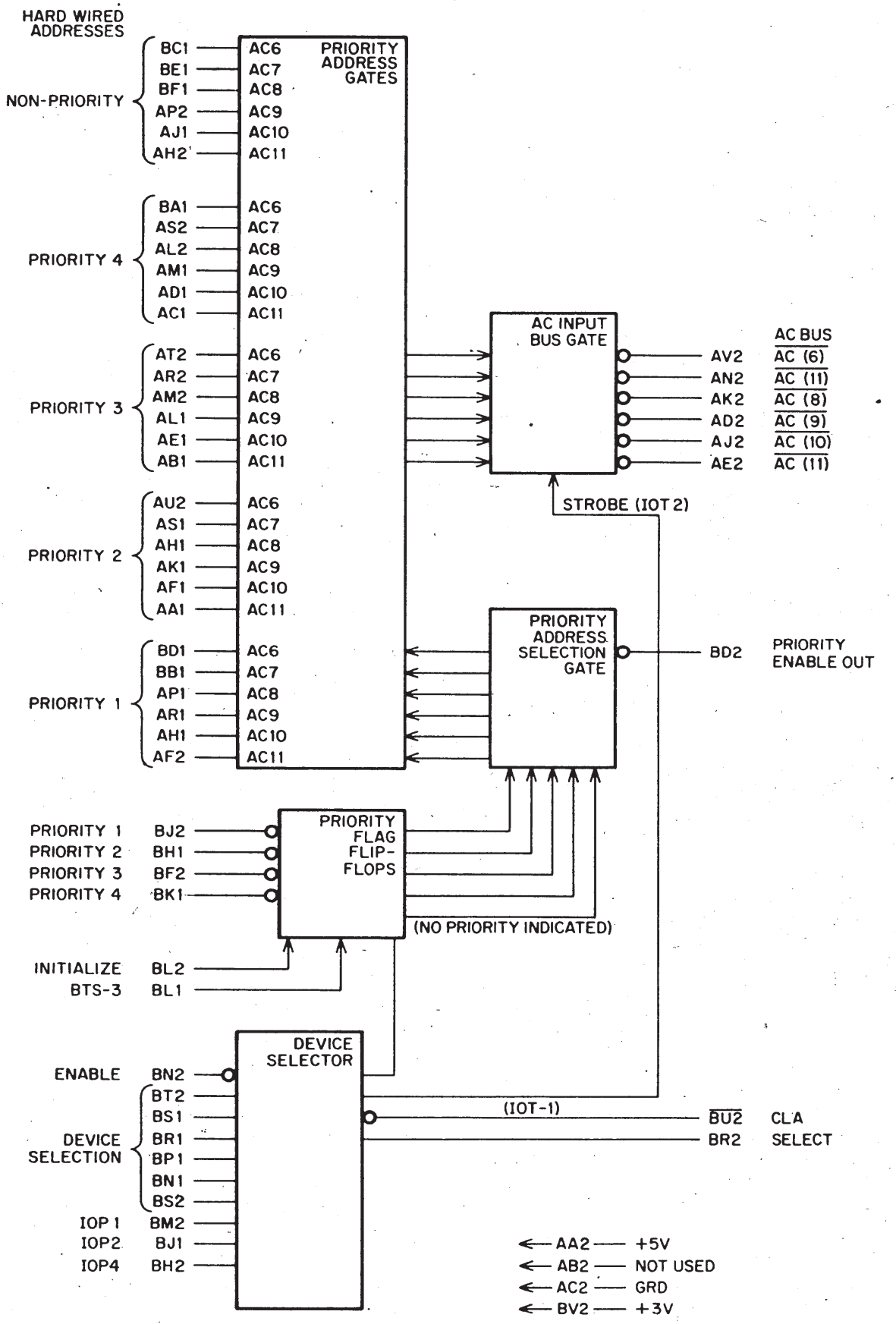
PRIORITY INTERRUPT MODULE
M736

M SERIES



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The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices. Priority assignment may be provided for more than four devices by using additional M736 modules for each additional group of four devices. All M736's in a particular priority system would utilize the same device code.

THEORY OF OPERATION

Basically the M736 module consists of the following:

1. The M103 device selector function.
2. A Bit Time State-3 (BTS-3) input.
3. Four priority input lines.
4. Priority enable line, input and output.
5. Five groups of six gates, each of which is capable of being hard wired to provide address information to locate subroutings to service the various devices associated with the priority interrupt system. The output of each of these gates is strobed onto the accumulator input bus on lines AC(6) thru AC(11).

SEQUENCE OF OPERATION

The external device activates its skip and/or interrupt FLAG flip-flop. The activation of the FLAG causes two things to happen; (a) The computer's interrupt request line is pulled to ground. This tells the computer that an external devices requires service and requests the computer to jump to an I/O priority interrupt service subroutine as soon as the computer completes its present cycle. (b) The external device FLAG pulls to ground the appropriate hard wired priority line connected to a "D" flip-flop in the M736.

A Bit Time State-3 (BTS-3) pulse from the computer is applied to the clock input of the "D" flip-flop to which the activating device flag is connected, as mentioned in section 1b above, and causes this flip-flop in the M736 to set. If more than one priority devices called to be serviced at the same time, all of the associated priority "D" flip-flops in the M736 would be set at this time. The outputs of the priority flip-flops in the M736 are connected to a priority gate structure which is arranged in such a manner that only one output line will be activated and that line will be associated with the external device with the highest priority.

This activated output of the priority gate structure is applied to one group of six two-input gates which make up the address gate. The other input of each of the six two-input gates of the address gate is hard wired to provide a discrete address which will correspond to the starting location of the particular

subroutine associated with that priority request. Each of the six output lines of the activated address gates is applied to one input of a two-input gate of the AC input strobe gate.

The computer now has had time to jump to the priority interrupt service routine and now issues a device selection code corresponding to the hard wired device selection code assigned to the M736 priority interrupt modules. This device selection code will pre-enable the IOP gates of the M736 of M736's.

The computer now issues an IOP-1 pulse to the IOP-1 gate of the M736 module. The output of the IOP-1 gate now produces an IOT-1 pulse which causes the "Clear the AC" line of the I/O bus to be pulled to ground, and thereby clears the AC.

The computer issues an IOP-2 pulse to the IOP-2 gate of the M736 module. The output of the IOP-2 gate produces an IOT-2 pulse which is applied to the strobe inputs of the AC input bus gate. As the other inputs of the AC input bus gate are connected to the outputs of the address gate, appropriate lines of the AC input bus (AC 6 thru AC 11) will be pulled to ground thereby loading into the AC the starting address of the subroutine associated with the particular priority I/O device to be serviced.

The computer now refuses to accept any further interrupt requests and jumps to the subroutine with the particular starting address which was loaded into the AC. The service routine of the particular priority device contains an instruction to clear the interrupt flag flip-flop of the particular I/O device and at the end of the subroutine issues the M736 device selector code with an IOP-4 which clears the priority flag flip-flops of the M736. The computer now turns on the priority interrupt system capability which allows the computer to service any future interrupt requests.

USING THE M736 PRIORITY INTERRUPT MODULES

1. Assign a device selection code to the M736 priority system and connect the device selection inputs of the M736 to the proper device selection lines to assure decoding for that code. If more than one M736 is used connect the device selection lines for each M736 in exactly the same manner. Each M736 will use the same device selection code.
   These inputs are: BT2, BS1, BR1, BP1, BN1 and BS2.
2. Connect the enable input, BN2, of each M736 to GRD.
3. Connect the IOP-1 input, BM2, to the IOP-1 bus line.
4. Connect the IOP-2 input, BJ1, to the IOP-2 bus line.
5. Connect the IOP-4 input, BL2, to the IOP-4 bus line.
6. Connect the BTS-3 input, BL1, to the BTS-3 bus line.
7. Connect the outputs of the external I/O device flag flip-flops to the priority

NOTE: In normal operation, IOP-4, is not required as the flag flip-flop in the external priority I/O device is cleared by the subroutine servicing that device. When the flag in the I/O device is cleared, the next BTSO3 pulse will load the disabled flag outpu tinto its respective priority flag flip-flop in the M736 effectively clearing the priority flag flip-flop. flip-flop.

inputs in such a manner as to pull the corresponding priority input line of the M736 to GRD when the device flag is activated. These inputs are as follows:

1st priority	BH1	"	"	"
2nd priority	BF2	"	"	"
3rd priority	BK1	2nd	"	"
4th priority	BJ2	"	"	"
5th priority	BH1	"	"	"
6th priority	BJ2	1st	M736	module

etc. carry on for additional priority interrupt devices.

8. Assign starting address to the subroutines which will service each priority interrupt device attached to the priority interrupt system. Also assign a starting address for the subroutine to service non-priority devices. Hard-wire the various starting address of the service routines as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 1	BD1	BB1	AP1	AR1	AH1	AF2
Priority 2	AU2	AS1	AN1	AK1	AF1	AA1
Priority 3	AT2	AR2	AM2	AL2	AE1	AB1
Priority 4	BA1	AS2	AL2	AM1	AD1	AC1
NON-Priority	BC1	BE1	BF1	AP2	AJ1	AH2

NOTE: If more than four external I/O devices require priority assignments, the NON-priority address inputs BC1, BE1, BF1, AP2, AJ1 and AH2 of the M736 module used for the first four highest priorities, *must* be connected to GRD. If more than two M736 modules are required all of the NON-priority address lines of each module except the last M736 containing the lowest priorities, must be connected to GRD. The NON-Priority address is hardwired to the NON-Priority address inputs of only the lowest priority M736 module. All un-used priority address inputs must be grounded. Logic 1 level for address may be obtained from module pin BV2 of each M736 module. Lower priority addresses would be hardwired on succeeding M736 modules in the same order hard wired to the second M736 module as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 5	BD1	BB1	AP1	AR1	AH1	AF2
Priority 6	AU2	AH2	AK2	AD2	AJ2	AE2

9. Connect the AC input bus gate outputs to the AC bus as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Module Pins	AV2	AH2	AK2	AD2	AJ2	AE2

10. Connect the Priority Enable input line BE2, of the M736 with the highest priorities, or the only priorities, to ground.

11. If lower priorities of 5 or more are assigned, connect the Priority output of the module with the higher priorities, Pin BD2, to the next M736 module (with the next following four lesser priorities) Priority enable input pin BE2.

12. Last, but not least, connect the INITIALIZE input, BL2 to the Initialize line of the computer I/O bus.

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