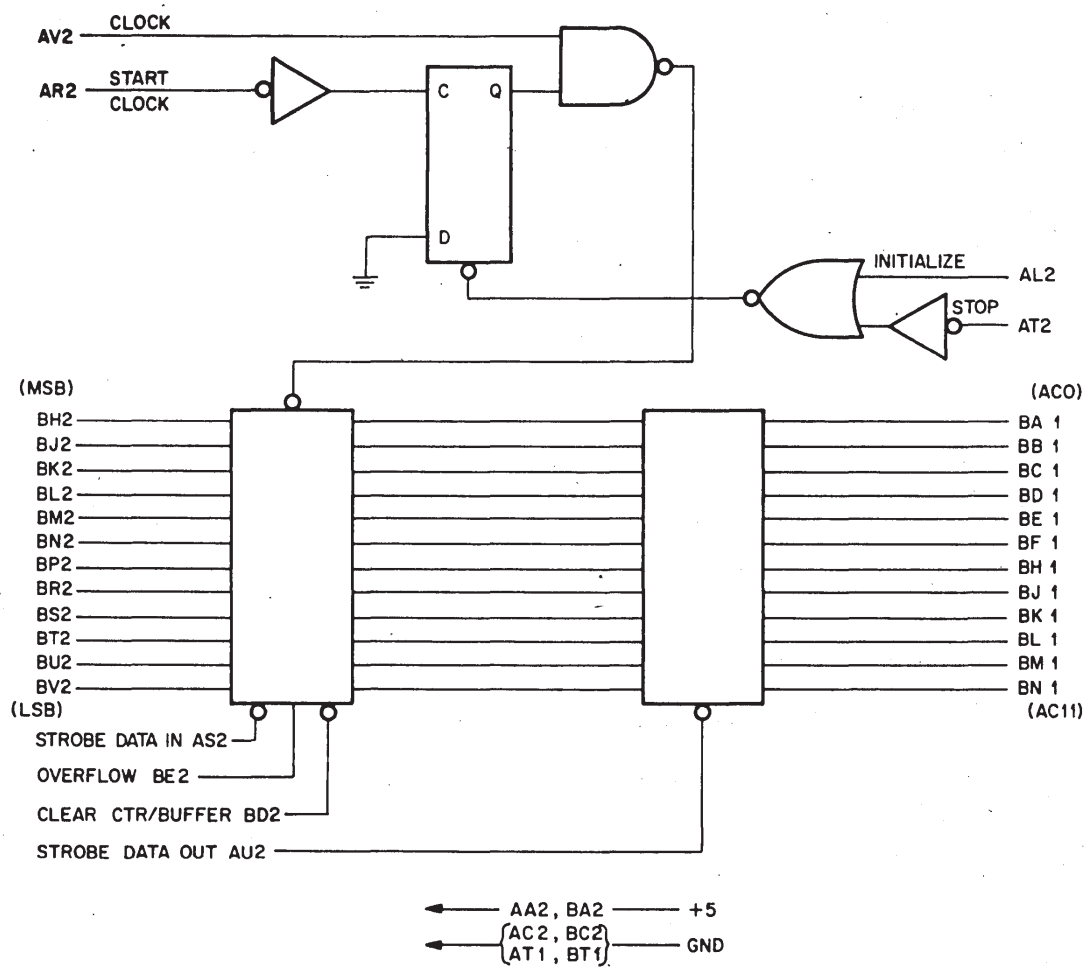
COUNTER-BUFFER INTERFACE
M738

M SERIES



The M738 Counter-Buffer Interface is contained on a double height, single width module.

The M738 was designed primarily to strobe twelve parallel bits onto the positive bus of the PDP-8/I or PDP-8/L. This module consists of three basic sections: 1) A twelve bit bus driver, 2) A twelve bit Up Counter which is presetable by jam transfer, and 3) A clock input gate circuit twelve bit bus driver.

The twelve bit bus driver is used to strobe the contents of the buffer counter onto the bus when a logic 0 (gnd) is applied to the "Strobe Data Out" pin AU2. The output of the bus driver consists of an open collector NPN transistor which allows the data outputs of other M738 modules to be parallel in a collector OR to ground fashion.

These outputs can sink 225 MA to ground and are protected against negative voltage undershoot in excess of −.9v.

The input to the "Strobe Data Out" pin AU2 would normally be an IOT pulse derived from a M103 or M107.

Twelve bit up counter-buffer:
The twelve bit counter-buffer consists of three MSI, 4-bit presetable counters connected in tandem. Twelve parallel bits of data may be applied to the data inputs and then jam transferred into the counter by the application of a logical zero of time duration equal to or greater than 250 n seconds to the "Strobe Data In" pin AS2. This input could be an IOT pulse from a M102 or M107.

The contents of the counter may be cleared by the application of a logical zero of time duration equal to or greater than three micro-seconds applied to the "clear counter/buffer" input pin BD2. The requirement of a three micro-second pulse precludes the direct use of an IOT pulse for clearing the counter. If it is required to clear the counter by the command of an IOT pulse, a M302 dual delay multivibrator could be used to stretch the IOT pulse length. At times, it may be desirable to connect two or more M738 module counters in tandem. This may be accomplished by connecting the "overflow" output pin BE2 of the first M738 to the "clock" input pin AV2 of the next M738. The clear pulse time duration should be an additional 3 micro-seconds for each M738 added in tandem; i.e. 24 bits would require a 6 micro-second clear pulse.

Clock Input Gate
The clock input gate circuit contains a storage flip-flop which serves to gate a clock pulse applied to the "Clock" input, pin AV2, into the counter buffer. This flip-flop may be initialized by the application of a logic one pulse (+ voltage pulse) to pin AL2 or by a logic zero (ground pulse) applied to the "Stop" input AT2. When the flip-flop is initialized, clock pulses applied to the clock input, pin AV2, will *not* be counted. Clock pulses may be counted by setting the flip-flop with the application of a logic zero pulse to the "Start Clock" input AR2. The four inputs, clock, start clock, stop and initialize require a minimum pulse width of 50 nanoseconds and therefore could use IOT pulses derived from the device selectors M103 or M107.

Inputs:
AS2 — 3TTL Loads
AU2 — 12TTL Loads
All other inputs — 1 TTL Load
(See text for timing considerations)

Outputs:
BE2 — 10TTL Loads

All other outputs consist of open collector NPN transistors which are capable of sinking 25 MA to ground. Voltage applied to these outputs must not exceed +20 volts. The outputs are diode protected against negative voltage undershoot in excess of −.9 volts.

Power:
+5v at 250 MA (maximum) — no strobe onto bus.
370 MA (maximum) — during bus strobe.

M738 — $105