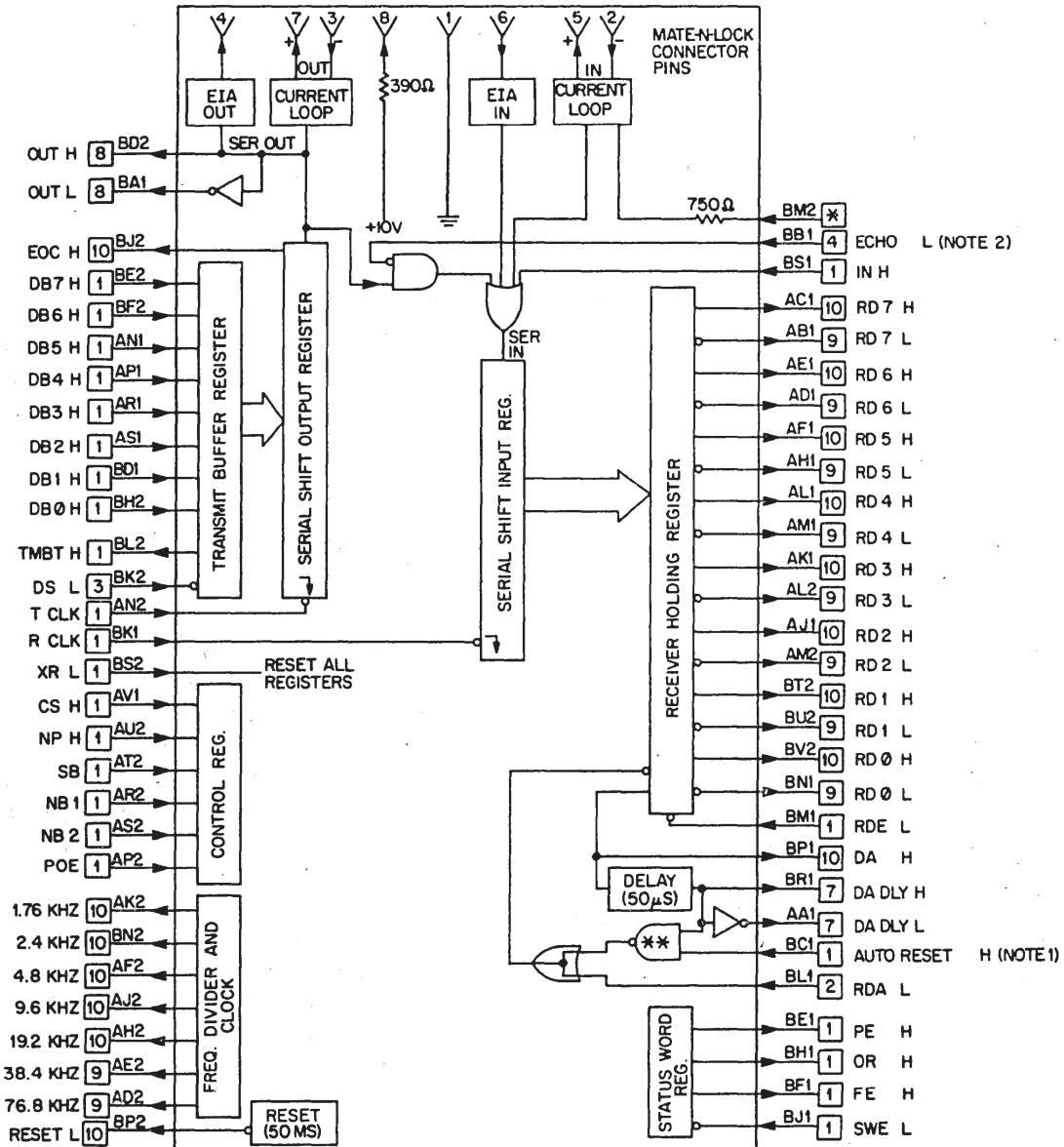# M7390
ASYNCHRONOUS TRANSCEIVER

Length: Extended
Height: Double
Width: Single

Price:

$275

NOTES: ✱=TIED TO −15V WHEN M7390 USED TO DRIVE CURRENT LOOP
✱✱=OPEN COLLECTOR OUTPUT
1. MUST BE TIED TO GROUND IF RDA L NOT USED
2. MAY BE LEFT OPEN IF ECHO NOT DESIRED

Volts	Power mA (max.)	Pins
+5	700	BA2
+10	3	AV2
GND		BC2
−12*	80	BR2
−15*	80	BB2

*Requires −12 V or −15 V only, not both.

DESCRIPTION

The M7390 asynchronous transceiver is a modular subsystem which provides asynchronous serial line compatibility for data communications applications. The M7390 combines input/output level converters, parallel-to-serial and serial-to-parallel conversion, and a crystal controlled clock, into one module.

APPLICATIONS

The M7390 can be used for computer terminal applications, data entry devices or any system which requires asynchronous serial line compatibility. The M7390 may also be used to drive modems conforming to EIA RS-232C specifications or current-operated devices such as Teletypes.

FUNCTIONS

There are three groups of functions on the M7390—error detection, data, and control.

Error Detection: The error function of the module allows three types of errors to be detected. These are:

1. Parity: If the received parity bit does not agree with the expected parity bit, the parity error flag is set.

2. Overrun: The receiver section of the M7390 is fully double buffered. Therefore, one full character time is allowed to remove the received data from the receiver buffer before a new character is assembled and transferred. If the character is not removed before a new one is loaded, the overrun flag is set.

3. Framing: Since the M7390 is asynchronous, the absence of a stop bit can be detected. For example, an eight bit data character would have one start bit, eight data bits, and one or two stop bits. Therefore, a stop bit is expected as the 10th bit to be received. If the 10th bit is in the logic TRUE (marking) condition no error is detected. However, if the 10th bit is a logic FALSE (spacing) condition, the framing error flag is set. The framing error flag is useful for detecting open lines or null characters.

Data Functions: The M7390 performs serial-to-parallel and parallel-to-serial conversion. The parallel side of the module is TTL compatible. The serial inputs and outputs are available as three signal sources: EIA, current loop or TTL. The current loop and EIA input and output are available only on the eight-pin MATE-N-LOK connector on the front of the module.

The EIA input corresponds to RS-232C specifications. In addition to the EIA signals RECEIVED DATA and TRANSMITTED DATA, the DATA TERMINAL READY signal and SIGNAL GROUND are also provided.

The current loop input/output is designed to operate on a 20 to 100 mA current loop. The M7390 uses optical couplers to provide 1500 volts of isolation between the M7390 ground and power and the driving source. The serial input will respond to a 20 mA current flow. Current flow is a marking condition (binary 1). The external source must not exceed 35 volts dc open circuit voltage or 100 mA current. The serial output is a transistor switch that can turn a current loop on or off. The open circuit voltage of the current source must not exceed 35 volts dc.

The TTL versions of the serial input and output signals are available on the module pins and may be used in place of the level converter signals.

Control: The M7390 provides full control of the receiver and transmitter sections. All control pulses must be greater than 250 ns in width. Data to be loaded into the module must be present 250 ns before the DATA STROBE pulse.

Receiver Control Signals:

DA	Data Available
DA DLY	Delayed Data Available
AUTO RESET	Allows DA to be automatically reset.
RDE	Receiver Data Enable. Places data and control signals on the pins of the module.
RDA	Reset Data Available

Transmitter Control Signals:

TBMT	Transmitter Buffer Empty
ECO	End of Character

Error Control and other Signals:

NP	No Parity
POE	Parity Odd or Even
SWE	Status Word Enable
CS	Control Strobe
NB1, NB2	Number of Bits in data word
SB	Number of Stop Bits (1 or 2)
XR	External Reset (clears all registers)
RESET	Negative pulse used for clearing module during power-up.
RCLK	Receiver Clock Input
TCLK	Transmitter Clock Input

PRECAUTIONS

1. EIA and current loop connections are available on an 8-pin MATE-N-LOK connector located in the handle position on the B half of the board.

2. Provision is made to power this module from either —15 or —12 volts dc. Do not use both simultaneously.

3. Current loop input and output circuits must not have more than 35 volts peak applied or greater than 100 mA current flow.

4. The M7390 contains an MOS LSI chip. Care must be taken in proper handling and grounding of the module to prevent damage to the MOS chip.

5. The +10 volt dc supply is required only if the EIA level converters are used, or if the module is going to be used as a current source.

6. If the M7390 is used as a current source, 20 mA additional current must be supplied by the —15 volt and the +10 volt power supplies.

SPECIFICATIONS

Data Format: Asynchronous, serial by bit, least significant bit first.

Input/Output Level (Serial):

1. EIA RS-232C: Binary 1 = −3 to −25 volts dc
   Binary 0 = +3 to +25 volts dc

2. Current Loop: Mark (Binary 1) = 20 to 100 mA current flow
   Space (Binary 0) = <3 mA current flow

3. TTL: Binary 1 = HIGH
   Binary 0 = LOW

Data Rates: 110, 150, 300, 600, 1200, 2400, 4800 Baud.

Character Format: One start, 5, 6, 7, 8 data, parity (if requested), one or two stop bits.

Clock Frequencies (kHz): 1.76, 2.4, 4.8, 9.6, 19.2, 38.4, 76.8

Input/Output Levels (Parallel): All TTL compatible.

MORE INFORMATION

Additional information is available by writing to:

> Logic Products Applications Group
> Digital Equipment Corporation
> 146 Main Street
> Maynard, Mass. 01754