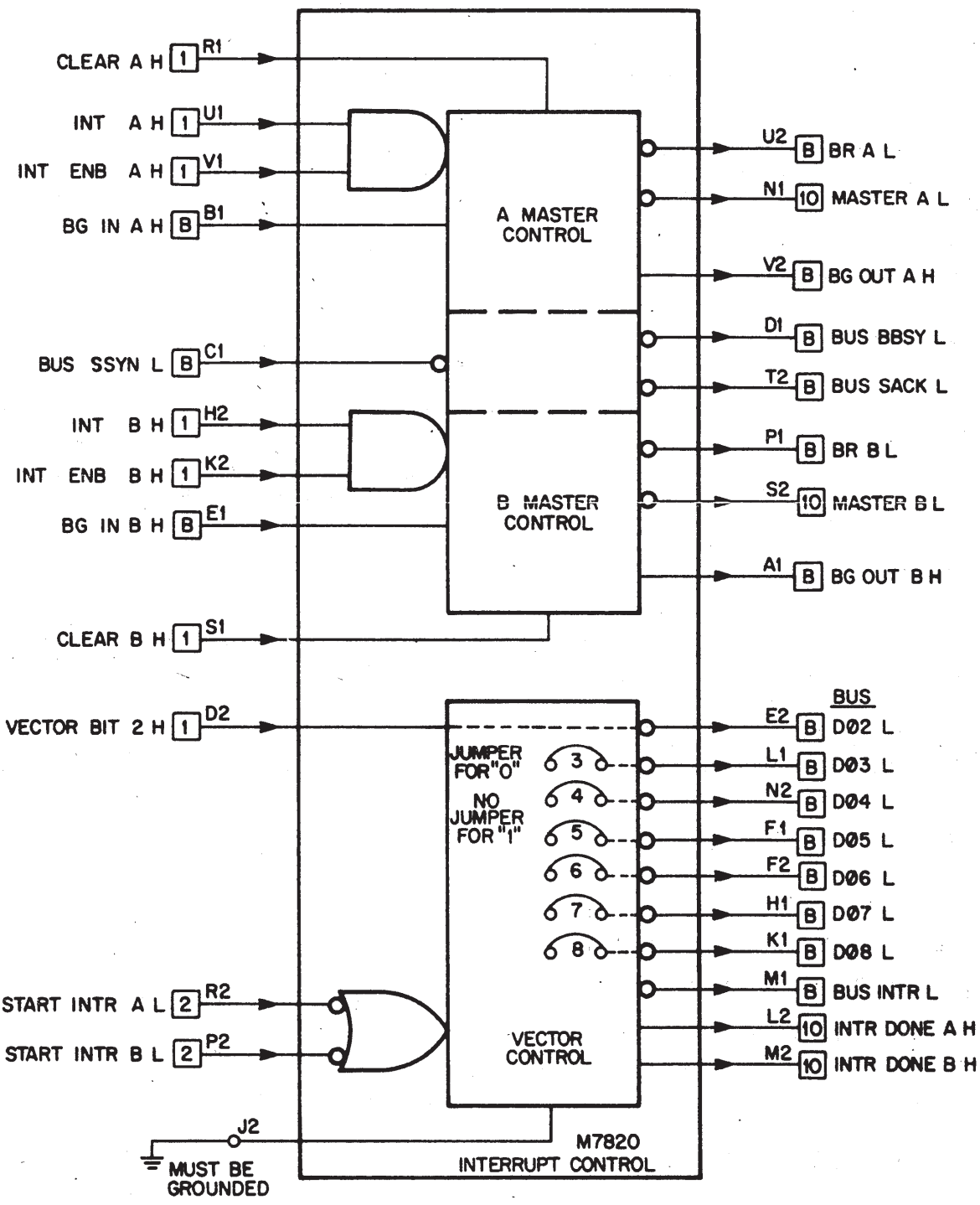
M7820
INTERRUPT CONTROL

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price: $100



Volts	Power mA (max.)	Pins
+5	290	A2
GND		C2, T1

The M7820 is used in PDP-11 device interfaces. It consists of logic circuits that can be divided into three functional sections: Master Control A, Master Control B, and INTR Control.

The Master Control circuits are used to gain control of the UNIBUS for satisfying the need to either gain direct memory access (DMA), or to perform the INTR bus operation which alters program flow.

To become master of the bus involves a question of priority. Briefly, this priority question is split into three phases: 1) bus request lines, 2) processor's priority level, and 3) physical placement of a device on the UNIBUS.

1) NPR (highest)
   BR7
   BR6 (except for trap instructions)
   BR5
   BR4 (lowest)

2) The processor acknowledges BR's of level $>$ N: where N is an Octal number in processor's status register. (NPR's are not affected.)

3) Highest priority goes to the device closest to the processor on the unique bus grant chain.

Theory Of Operation

If a device wants control of the bus, it asserts both INT A and INT ENB A. Then a request is made on a BR. This then leads to priority determination and a BG results. Now the Master Control A responds with BUS SACK. The processor sees this acknowledgement and removes BG. When BUS BBSY and BUS SSYN are negated, the Master Control A removes its BR and asserts BUS BBSY itself. It also asserts Master A when it is in control of the bus. Now the device can use the bus. To release control of bus, the device can assert CLEAR A or negate: INT A or INT ENB A. Master Control B is identical to A.

The INTR operation transfers a "vector address" to the processor. At this address is stored two consecutive words: 1) The starting address of the interrupt service routine, and 2) A status word. When the processor detects this, a trap sequence is initiated (current value of PC and current status of PS are stored and new ones are fetched). Now the interrupt service routine is executed.

To start the process: START INTR A or START INTR B is asserted. Then BUS INTR is asserted along with a 7-bit address. This is transferred onto the data lines: BUS D <08:02> providing a range of 000 to 374 (OCTAL) in increments of 4. D <08:03>are controlled by jumpers, which when "in," force the bit to zero. The processor seeing BUS INTR asserts BUS SSYN. When this is detected, an INTR DONE A is asserted which negates the START INTR signal. This in turn negates BUS INTR, which negates BUS SSYN. As a result, a trap sequence is initiated. Vector bit 2 controls D02. When it is asserted D02 is asserted. It does not control any other bits.

The grant chain to tie in the Master Control is as follows:

BG IN has 390Ω to GND and BG has 180Ω
+5 Volts.

EXT GND is used for testing purposes and should be tied to ground in normal operations.