

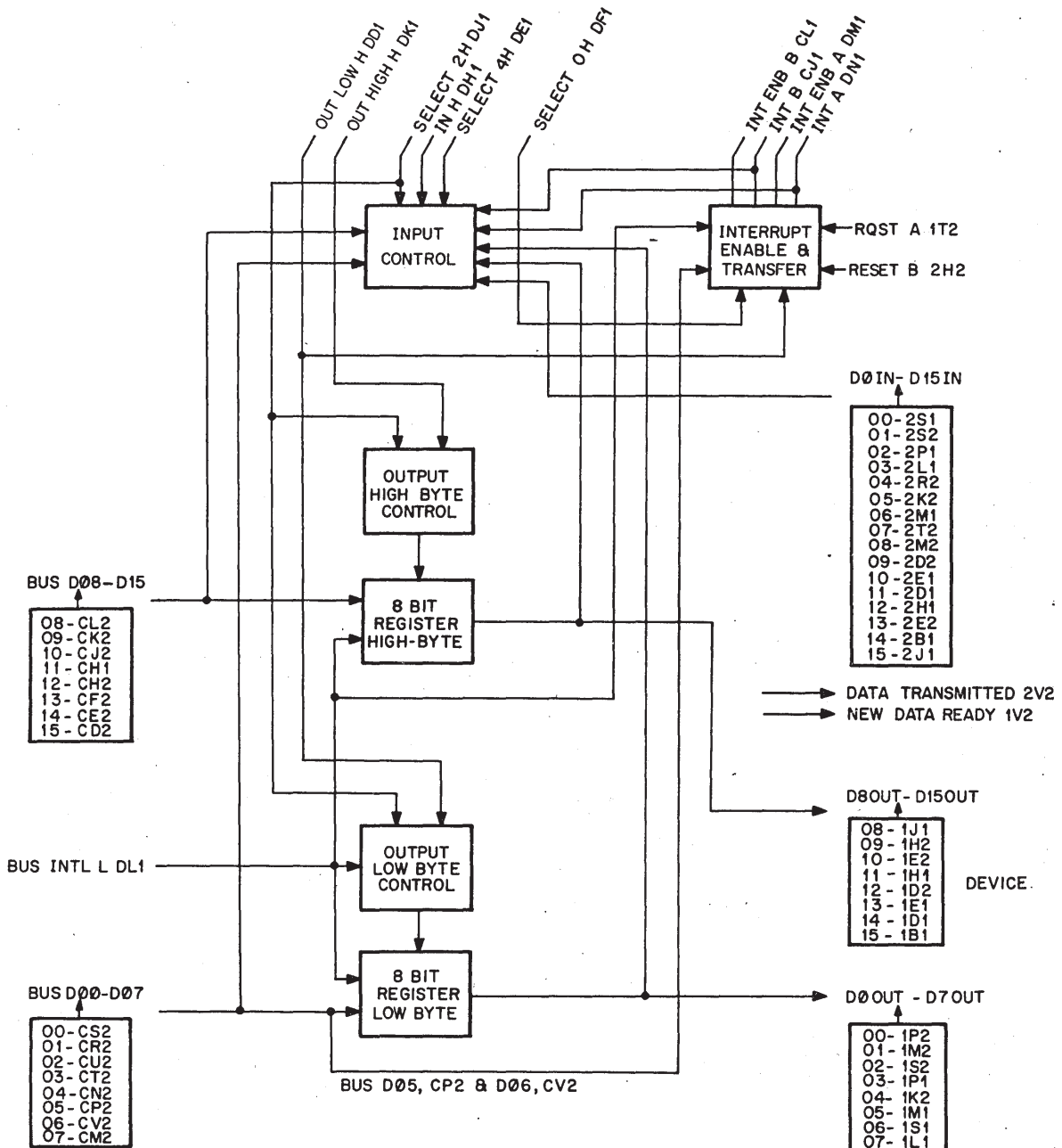
# M786 DEVICE REGISTER INTERFACE

**PDP-11  
UNIBUS**

**M SERIES**

**Length:** Extended  
**Height:** Double  
**Width:** Single

**Price:**  
  
**\$220**



Volts	Power	Pins
+5	mA (max.)	AA2, BA2
GND	600	AC2, BC2
		AT1, BT1

The M786 is a PDP-11 interface module containing all the logic necessary for transfers of 16-bit input and output data between a PDP-11 system and an external device. All I/O connections are made using the connector blocks mounted on the module.

## APPLICATIONS

For interfacing to the PDP-11, the M786 must be used with the M105 Address Selector. The M105 decodes the UNIBUS address lines and causes transfer of information through the M786 module under program control. Interrupt circuitry is also built into the M786 module and can be used in conjunction with the M7820 module or equivalent. An example of a typical PDP-11 interface using the M786 module is illustrated in Figure 1.

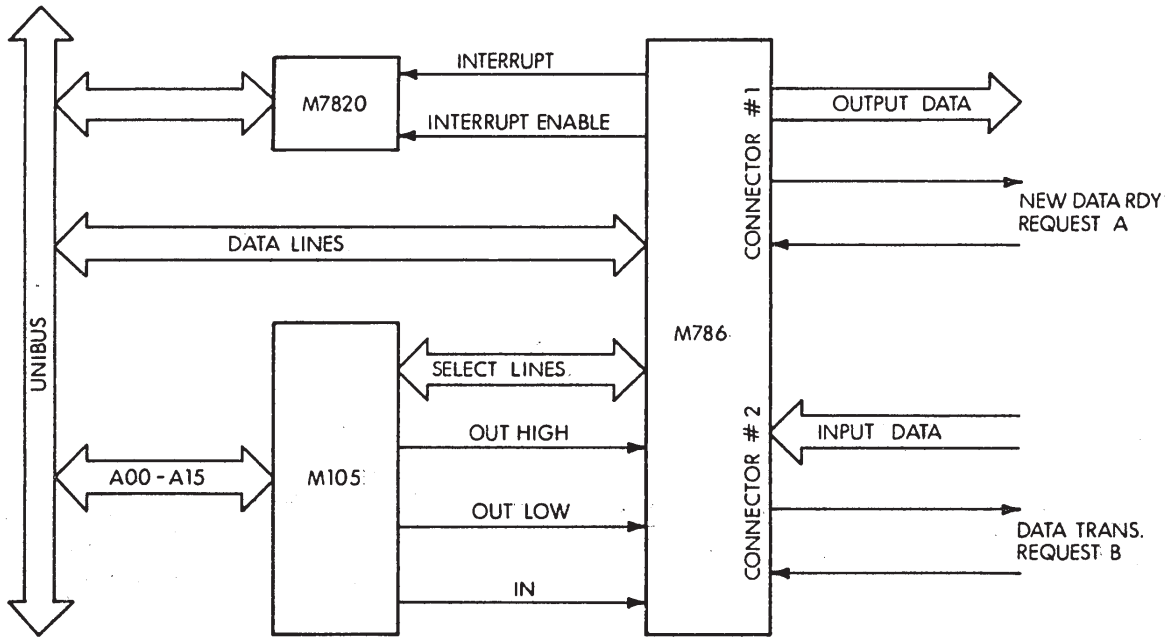


Figure 1. Typical PDP-11 Interface

## FUNCTIONS

**Registers:** The M786 module contains a 16-bit register interfaced to the computer bus data lines by ungated receivers. Data from the computer is clocked into the registers by strobing signals OUT LOW with SEL 2 and OUT HIGH with SEL 2 derived from the M105 module. The user has the option of reading whole words (OUT LOW with SEL 2 and OUT HIGH with SEL 2) or 8-bit bytes (OUT LOW with SEL 2 for a low byte and OUT HIGH with SEL 2 for a high byte). All register outputs go to I/O connector No. 1 where cables from an external device can be attached.

The M786 module signals the external device through the NEW DATA signal each time new data is loaded into the 16-bit register. Register outputs may be read back onto the computer bus by program-enabling the IN 4 and SEL 2 signals from the M105 module.

**Drivers:** Sixteen bits of TTL data may be received from an external device via cables attached to I/O connector No. 2. These input lines are protected by clamping diodes to prevent input signal swings above or below the normal TTL levels. Each of these input signals can be read onto the computer bus by means of bus drivers which are enabled by the IN H and SEL 4 signals from the M105 module.

The M786 module signals the external device through the DATA TRANSMITTED signal that data has been read onto the computer bus.

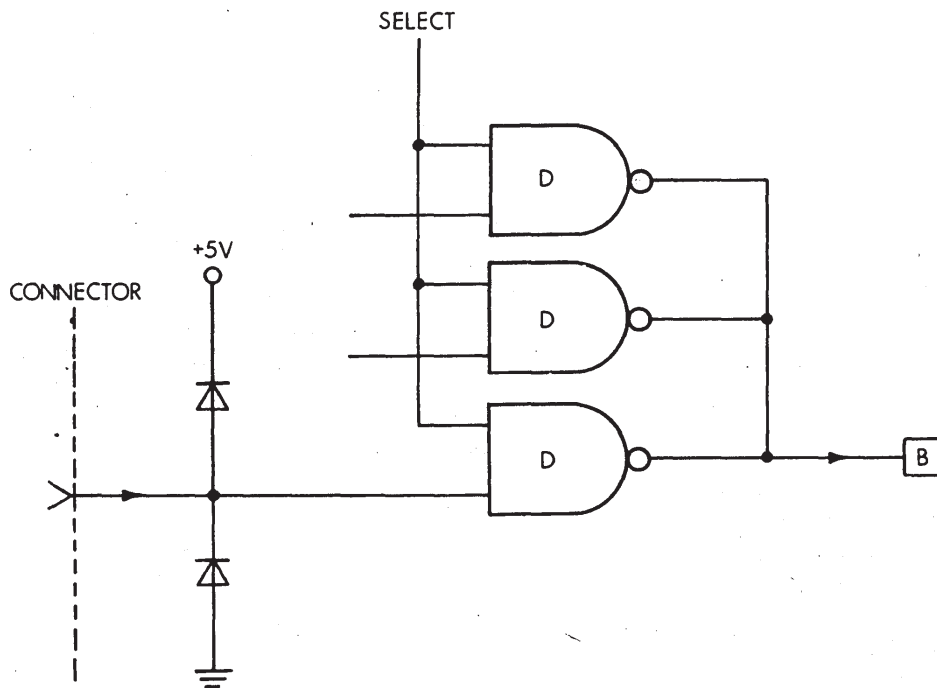


Figure 2. Typical Input Circuit

**Interrupt:** Each I/O connector also has an additional request line (REQUEST A on connector No. 1, REQUEST B on connector No. 2) which may be asserted High by the external device to initiate an interrupt or to generate a flag that may be tested as part of a peripheral status-checking program. Whether these two request lines cause an interrupt is determined by two Interrupt Enable flip-flops (INTR ENB A, INTR ENB B) which may be set under program control to enable interrupt capability for either an A or B interrupt or both if dual interrupts are required.

For interrupt capability, an INTR ENB and a REQUEST signal are applied to an M7820 module or equivalent. These two signals must be both A or B signals; for example INTR ENB A and REQUEST A.

The priority level of both interrupts on the M786 module must be the same, with the interrupt which is back panel-wired closest to the processor having the highest sublevel priority. The M786 module contains a priority jumper plug which is normally set at BR5. If other priorities are desired, different plugs may be purchased.

**Status Gates:** Status gates on the M786 module give the programmer the ability to check the states of the REQUEST and INTR ENBL signals. These gates are software-enabled through the address selector (M105 module) signals SEL 0 and IN H.

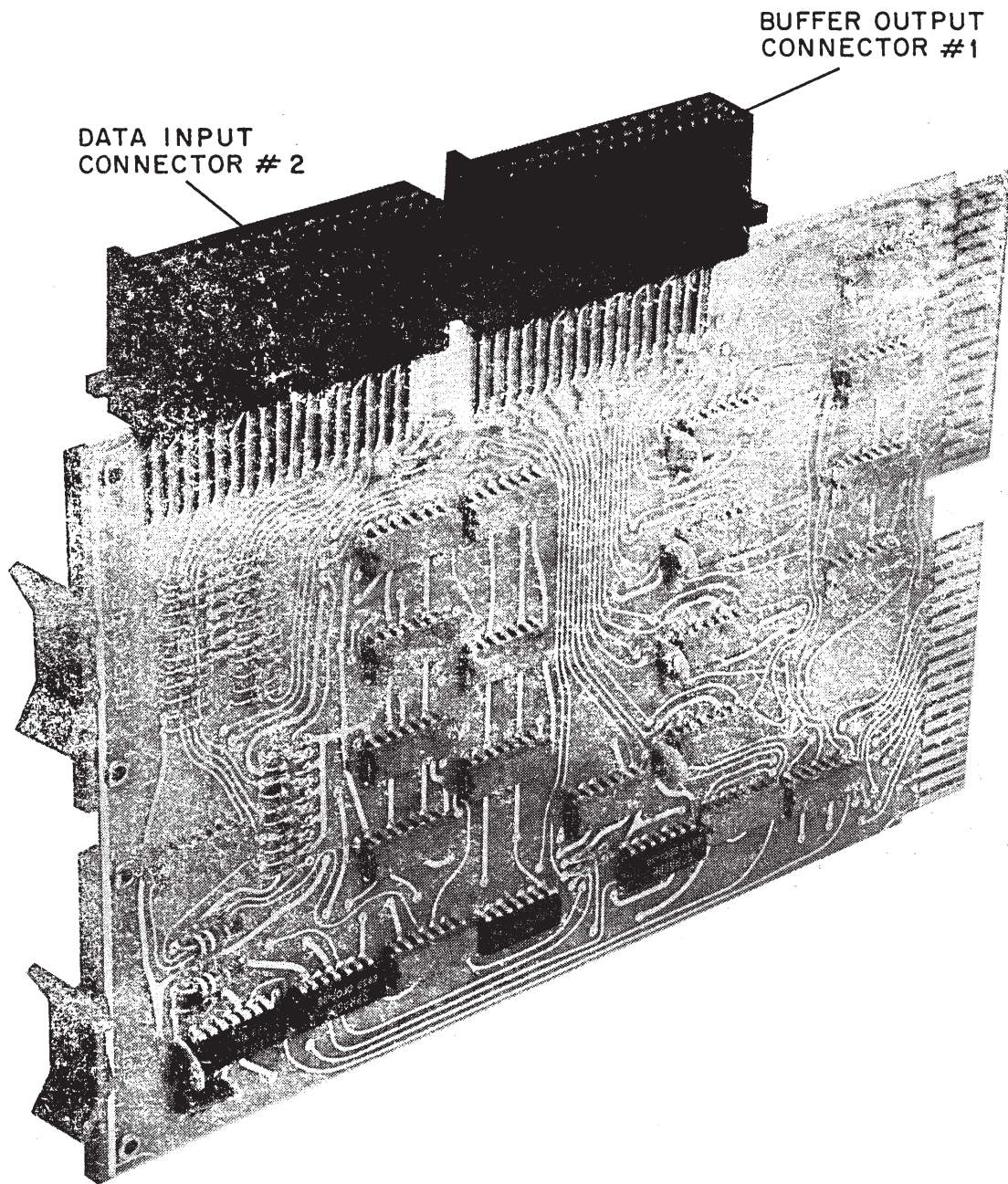
## SPECIFICATIONS

### Propagation Time:

FROM	TO	ns (max)
Bus DATA	I/O Connector	100
I/O connector	Bus DATA	35
Flag Clock Inputs	Flag output	40

### I/O Connector Cables:

The I/O connector accepts the M904 and M927 Cable Connectors which contain solder lugs and can be used with ribbon cable, twisted pair cable, or open wire.



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