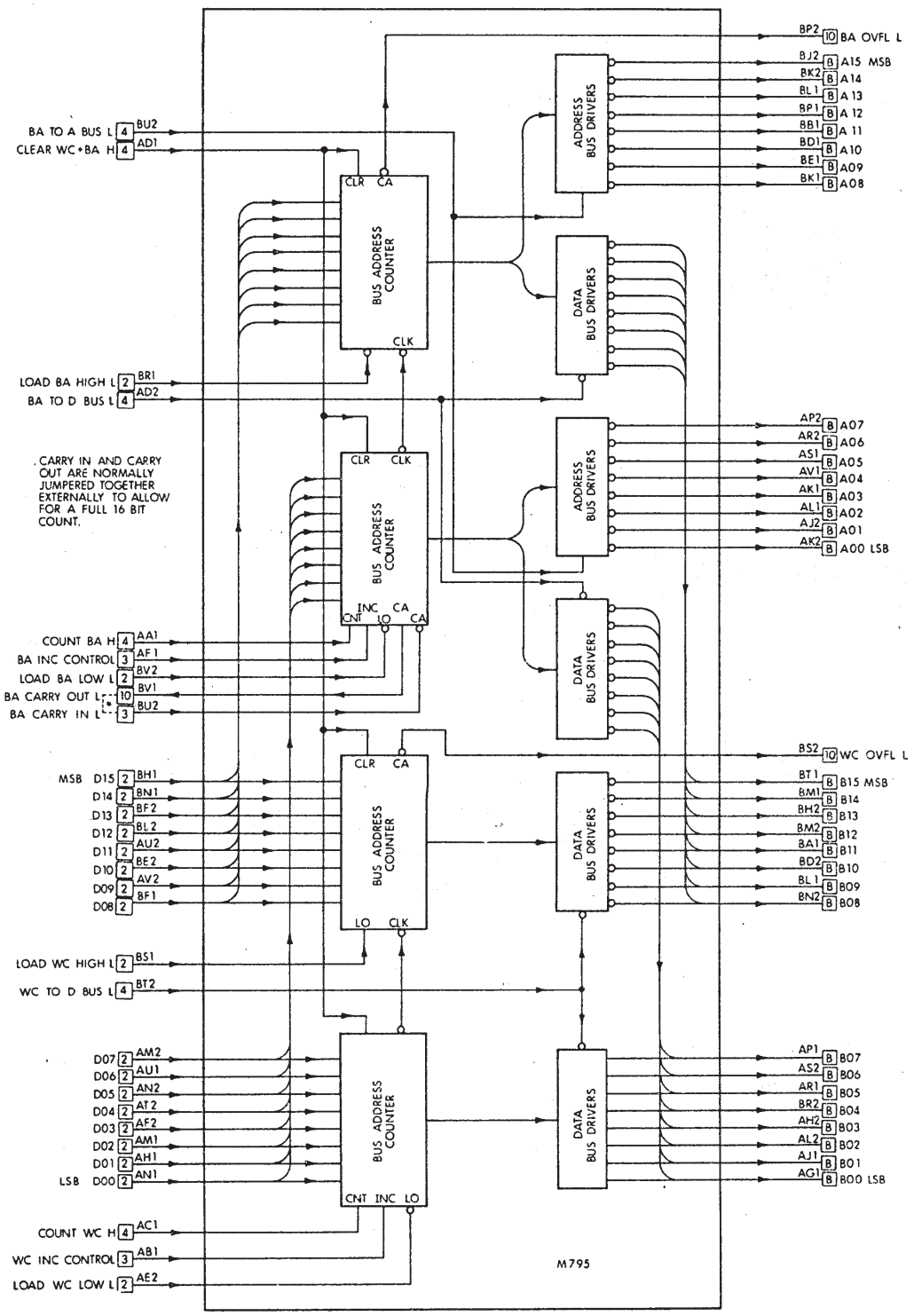
M795
WORD COUNT AND BUS ADDRESS MODULE

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single

Price: $200



Volts	Power mA (max.)	Pins
+5	600	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M795 Word Count and Bus Address Module is used to interface Direct Memory Access (DMA) devices to the UNIBUS. This module contains two 16-bit counters. One counter is used to count the number of data transfers that occur. The other counter is used to specify the bus address of the data to be transferred.

FUNCTION

Word Counter

Block transfer devices that function as bus master during data transfers usually require two registers to hold the parameters of the transfer. One parameter is the transfer word count. Initially, this register (WC) is loaded with the 2's complement of the number of items to be transferred to or from memory. This number is placed on the BUS DATA lines (D00-D15) and clocked into the WORD COUNT register in two 8-bit bytes using the LOAD WC L (low byte) and LOAD WC + 1 L (high byte) inputs. After each data transfer is complete, the WC register is incremented by clocking the COUNT WC H input. If the new value of the WC register is 0 which is indicated by an overflow at the WC OVFL L output, further transfers are inhibited and the block transfer is complete. Information can be transferred in either words (16 bits each) or bytes (8 bits each), because the WC register may also be used as a byte counter.

Address Counter

The second parameter used in block transfers is the transfer address. Initially, a bus address register (BA Counter) is loaded with an address that specifies the memory location to or from which data is to be transferred. This address is loaded from the BUS DATA lines (D00-D15) in two 8-bit bytes using the LOAD BA L (low byte) and LOAD BA+1 L (high byte) inputs. The BA register is incremented after each transfer by clocking the CLOCK BA H input. The register continually "points" to sequential memory locations.

BUS Drivers

Outputs of both the Word Counter and BA Counter are connected to a set of UNIBUS drivers so that the counter contents can be gated to the DATA BUS when the appropriate enable signals (BA TO BUS L and WC TO D BUS L) are asserted. In addition, the BA register has a set of drivers with independent outputs to allow it to drive the ADDRESS BUS when the BA TO BUS L input is asserted.

Counter Increments

The BA register can be incremented by either 1 or 2 as a function of the BA INC CONTROL input (High=1, Low=2). This incrementation capability allows addressing of either sequential bytes or words. The register is incremented on the trailing edge of a positive pulse applied to the COUNT BA H input of the register. The carry between bits 03 and 04 is broken and brought out to pins BV1 (BA CARRY OUT L) and BU1 (BA CARRY IN L). Normally these pins are connected together externally to allow for a full 16-bit count. They can, however, be controlled to inhibit the carry and to force repeated addressing of 16 sequential byte addresses. This feature can be used in device-to-device transfers. An overflow pulse (BA OVFL L) is provided as an output whenever the register is incremented from all 1's to all 0's.

The WC register is incremented by either 1 or 2 as a function of the WC INC CONTROL input (High=1, Low=2). The register increments on the trailing edge of a positive pulse applied to the COUNT WC H input of the register. An overflow pulse is also available at pin BS2 (WC OVFL L). Both registers reset to 0's whenever the CLEAR WC+BA H signal is asserted.

The storage elements on the M795 module are not edge triggered devices. Data must be established and held for the duration of the loading pulse.

APPLICATIONS

This module is used to interface direct memory access (DMA) devices to the UNIBUS.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
CLEAR WC+BA	WC+BA Outputs	125
LOAD WC L	WC Outputs	75
LOAD WX+1 L	WC Outputs	75
COUNT WC H	WC Outputs	60
LOAD BA L	BA Outputs	75
LOAD BA+1 L	BA Outputs	75
COUNT BA H	BA Outputs	60