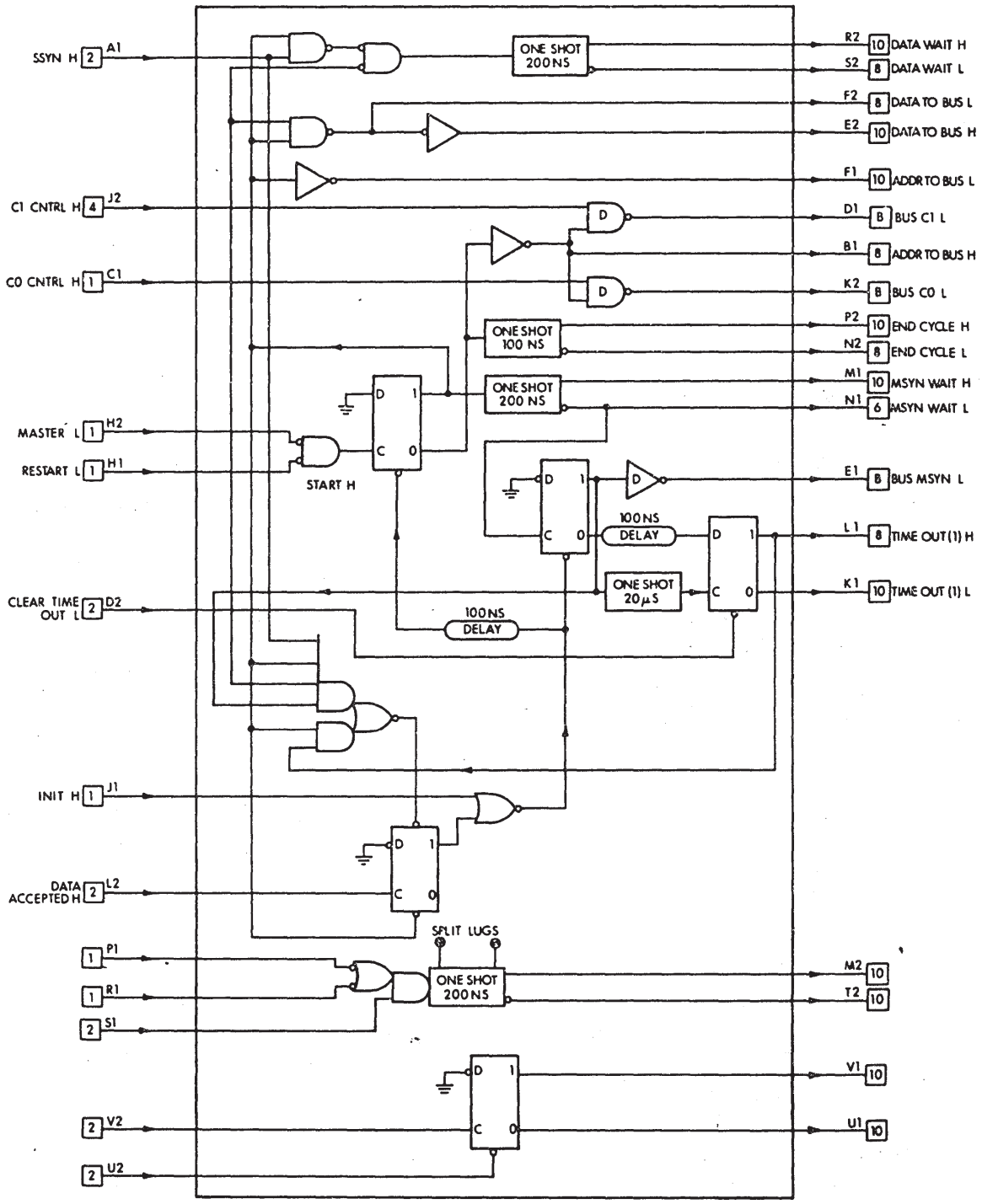
M796
UNIBUS MASTER CONTROL

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price: $100



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M796 UNIBUS Master Control Module provides extremely flexible control operations on the UNIBUS when a device is functioning as bus master. In addition to controlling the four transfer operations (DATI, DATIP, DATA, and DATOB), the M796 module generates strobe and gating signals which transfer both addresses and data to and from the bus; handles deskewing of data received from the bus; protects against data transfers to nonexistent devices by the use of time-out circuits; and provides a flip-flop and integrating one-shot that can be used by the customer for special control functions.

Any device in the PDP-11 system may have the capability of gaining control of the bus and, as bus master, of transferring data to and from other slave devices on the bus. This operation is performed independently of processor control and is usually referred to as Direct Memory Access (DMA). The logic necessary to gain control of the UNIBUS is provided by either the M7820 or M7821 Interrupt Control modules.

Upon becoming bus master, the device is free to conduct a data transfer. A DATI cycle is performed if the device needs data (either a word or byte) from memory; a DATO cycle is performed if the device is storing a word of data in memory (DATOB cycle for byte storage); a two-cycle DATIP, DATO(B) operation is performed if data held in memory is to be modified as in the case of increment memory or add to memory functions.

In order to execute one of these transfer cycles, the M796 must set Bus C0 and Bus C1 for the required type of data transfer, assert the MSYN signal, and then wait for the SSYN response from the slave. Data must either be gated to the Bus data lines on a DATO cycle or be received and strobed at the proper time on a DATI cycle.

The Bus C1 and Bus C0 outputs of the M796 can directly drive the UNIBUS and are asserted as a function of the control inputs C1 CNTRL H and C0 CNTRL H. Table 1 lists the states of the control inputs for the four possible bus cycles.

Table 1. Control Line Input States for M796

C1	C0	Bus Cycle
L	L	DATI
L	H	DATIP
H	L	DATO
H	H	DATOB

The data transfer sequence is triggered by meeting the AND condition of both Lows and RESTART L (HI). Usually these two inputs are tied together and are connected to the MASTER L signal produced by the M7820 or M7821 Interrupt Control Module. When the AND condition is met, it produces the START signal, which is an internal signal in the M796 module. At the transition of the START signal, both Bus C1 and Bus C0 are asserted as determined by their respective control inputs. The ADRS to Bus signals are also asserted and are used to gate the address of the slave onto the bus address lines (Bus A 17:00). If an output cycle is specified (C1 — 1), the DATA TO BUS signals (both H and L) are also asserted and are used to gate data to be transferred to the slave onto the bus data lines (Bus D 15:00). The MSYN WAIT one-shot outputs are asserted for 200 nanoseconds after START becomes true and are used to clear the interrupt request flags in the master device. When the MSYN WAIT one-shot times out, the BUS MSYN L signal is asserted. The master device then waits for a response from the slave.

In a data output cycle (DATO), assertion of SSYN causes BUS MSYN to be negated immediately. After a 100-nanosecond delay, BUS C1, BUS C0 ADRS TO BUS and DATA TO BUS are negated. When these signals drop, the END CYCLE pulse appears and is usually used to release control of the bus.

In a data input cycle (DATI), the assertion of the SSYN input produces a 200-nanosecond pulse that appears as DATA WAIT. This delay allows time for the incoming data to deskew and settle. The trailing edge of the DATA WAIT pulse can be used to clock data from the slave into the master device. If a strobe pulse is necessary, the trailing edge of DATA WAIT can be used to trigger the one-shot provided on the module. In either case, once data is received, a positive-going edge is applied to DATA ACCEPTED L causing BUS MSYN to be negated initially, followed by negation of ADDR TO BUS, BUS C1, and BUS C0 100 nanoseconds later.

A TIME-OUT flip-flop is set if a SSYN response fails to occur within 20 microseconds after BUS MSYN is asserted. When this flip-flop is set, the bus cycle is not performed. The TIME-OUT flip-flop is cleared by asserting the CLEAR TIME OUT L input.

The M796 module provides a special flip-flop that has the clock (V2), reset (U2), 1 side (V1) and 0 side (U1) available to the customer. The flip-flop is clocked by a positive transition on the clock input.

An integrating one-shot is also provided on the module. This one-shot is triggered whenever the output of the gating input becomes true: $(\overline{R1} + \overline{P1}) - S1$. The output pulse width at pins T2 and M2 is 150 nanoseconds but can be lengthened by adding capacitance across the pair of split lugs on the module. The following equation can be used to determine the approximate value of the added capacitance:

$$T_{pw} = 0.32\ (RC)$$

where T_{pw} is in milliseconds, R is in ohms, and C is in microfarads. (The internal resistance is 5.6 kilohms.)

Note that all times mentioned above represent nominal values with a tolerance of $\pm$ 25%. The delays and pulses provided by the module are controlled by simple RC circuits: therefore, if the user has any special requirements, part substitutions can be made to alter these time constants.