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- 40 Unused

Must tie either S or S<sub>+</sub> to GND if no DL8i  
Need a proper jumper list for dl8i, like those below.

EAE Disable Jumpers (blue wire wrap):  
(from Dave Gesswein)

- E28L1 to GND EAE\_L\_DISABLE
- F23H2 to +3 volts EAE\_E\_SET
- F24C1 to +3 volts EAE\_NO\_SHIFT\_ENABLE
- F28R1 to +3 volts EAE\_ON
- F31D2 to +3 volts EAE\_MEM\_ENABLE
- F33P2 to GND B EAE\_ON
- F39F1 to GND MQ\_ENABLE
- F39F2 to GND SC\_ENABLE

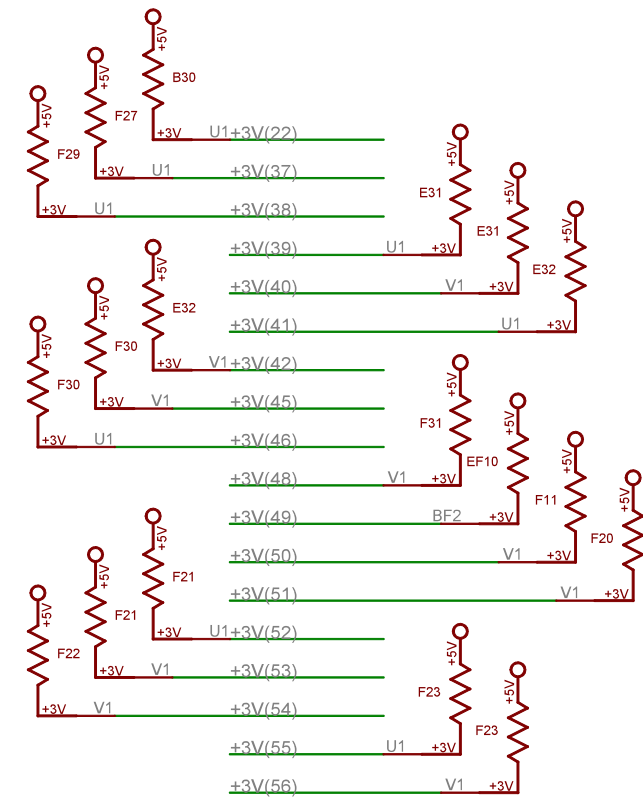
KT8i Disable Jumpers (blue wire wrap):  
(from Dave Gesswein)

- E13D1 to E15M2, UF(0) to +3V
- E18U1 to B4V1 SKIP ored to SKIP(1)
- F11M2 (or possibly F11H2 or F11N2) to F11U1, CUF to +3V
- F19N1 to F19N2 UINT to +3V
- J13U2 to H13P2 ME5 to +3V

Unused Slots:

- |     |             |
|-----|-------------|
| E03 | H06         |
| E04 | F04 H21 J21 |
| E05 | F05 H22 J22 |
| E06 | F06 H33     |
| E07 | F07 H35 J35 |
| E08 | H36 J36     |
|     | H37 J37     |
|     | H38 J38     |
|     | H39 J39     |
|     | H40 J40     |

BUGBUG: TP4 seems hopelessly overloaded, given that clock inputs are 2 standard TTL loads.



BUGBUG: This was done based on proximity, ignoring issues of authenticity. (Fanout has been checked.)



This kludge added by VRS, since IO\_PC\_LOAD isn't driven.  
This signal was added by an ECO, but lacks a driver.  
I've added a connector pin here, for now.

ECOs Believed to be Integrated:

- 8i-00001
- 8i-00002
- 8i-00009
- 8i-00013
- 8i-00015
- 8i-00020
- 8i-00021
- 8i-00025
- 8i-00029
- 8i-00034
- 8i-00042
- 8i-00046
- 8i-00050
- 8i-00054 Buffer MEM\_START and TP2.
- 8i-00059
- 8i-00067
- 8i-00069
- 8i-00071
- 8i-00081
- 8i-00084
- 8i-00085 Delay TP3 50ns so slow MM can meet set up for adder.
- 8i-00086

Other ECOs Known to Exist:

- 8i-00024 D-MU-8i-0-16 Module Utilization
- 8i-00026 D-CS-8i-0-27 Console switches and Indicators
- 8i-00032 D-MU-8i-0-16 Module Utilization
- 8i-00052 D-MU-8i-0-17 Module Utilization
- 8i-00068 D-MU-8i-0-17 Module Utilization
- 8i-00093 D-MU-8i-0-17 Module Utilization
- 8i-00096 D-MU-8i-0-17 Module Utilization
- 8i-00099 D-MU-8i-0-17 Module Utilization



Notes and Table of Contents

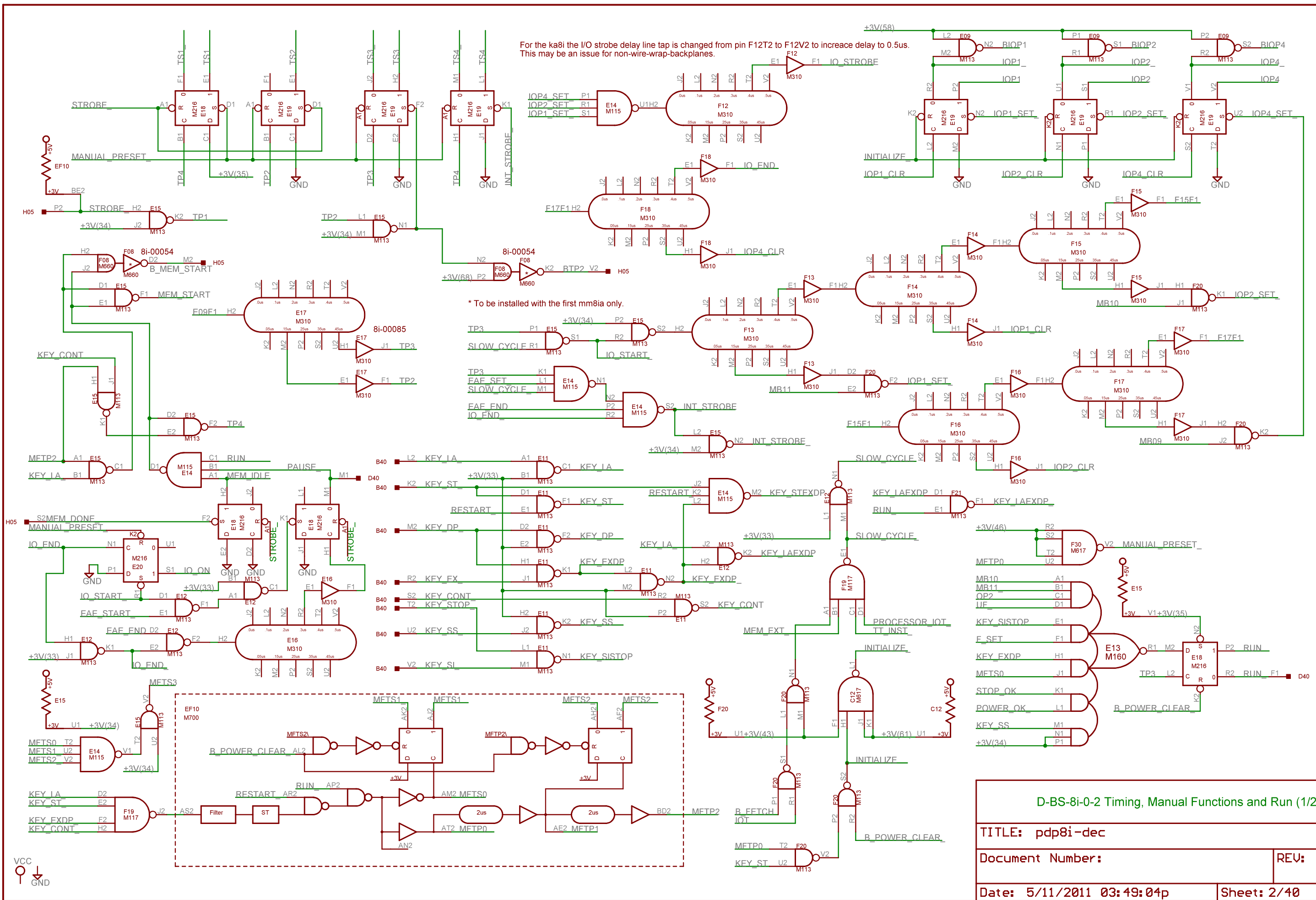
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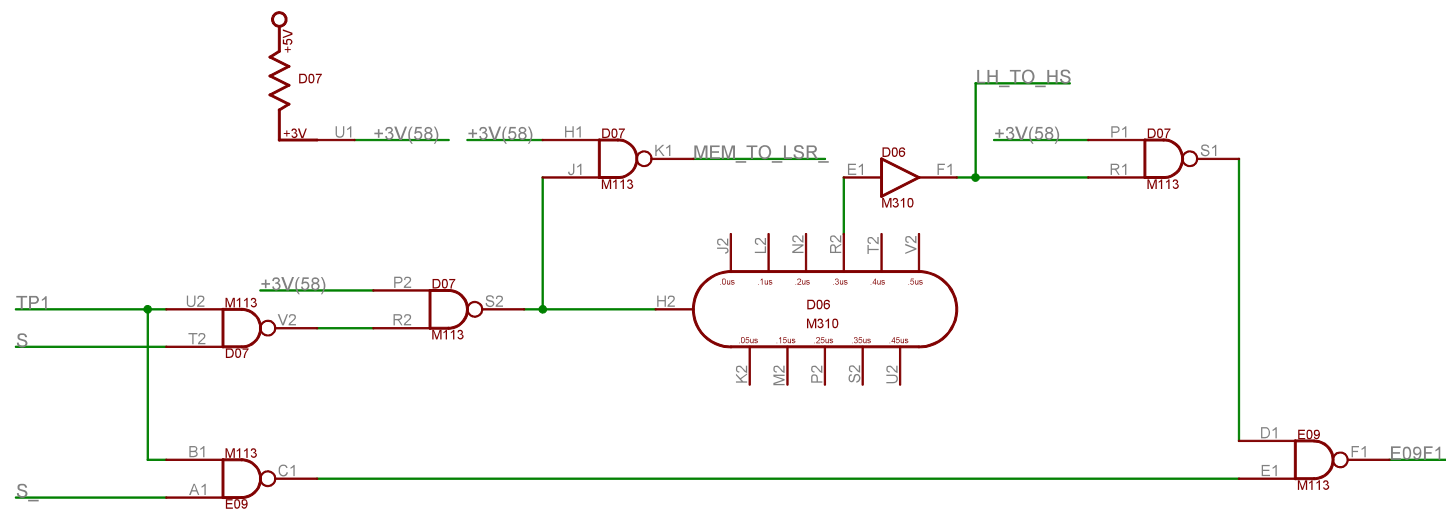


For the ka8i the I/O strobe delay line tap is changed from pin F12T2 to F12V2 to increase delay to 0.5us. This may be an issue for non-wire-wrap-backplanes.

\* To be installed with the first mm8ia only.

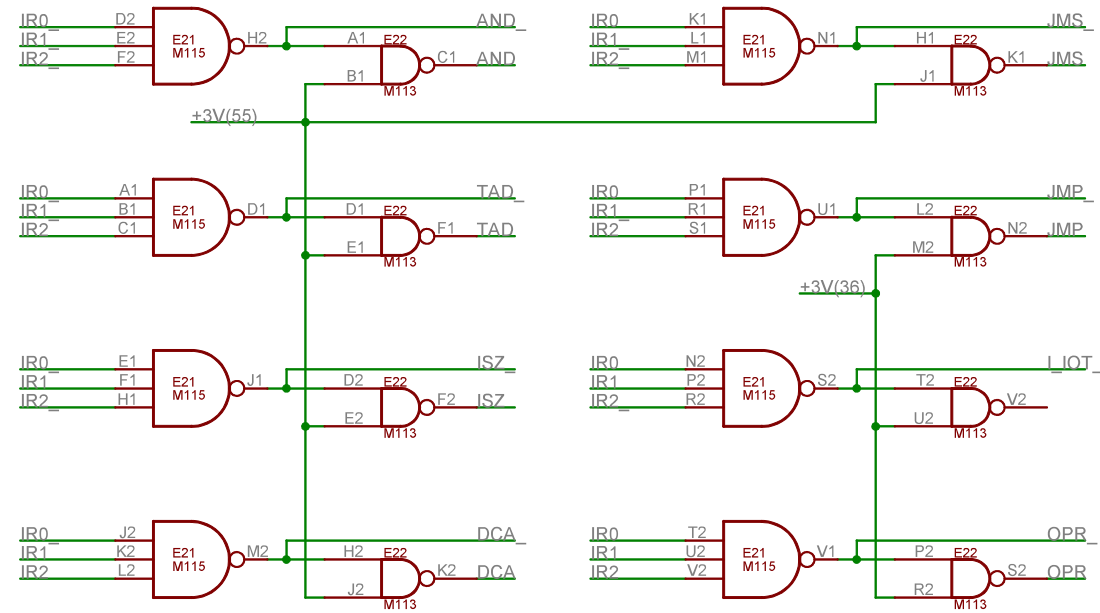
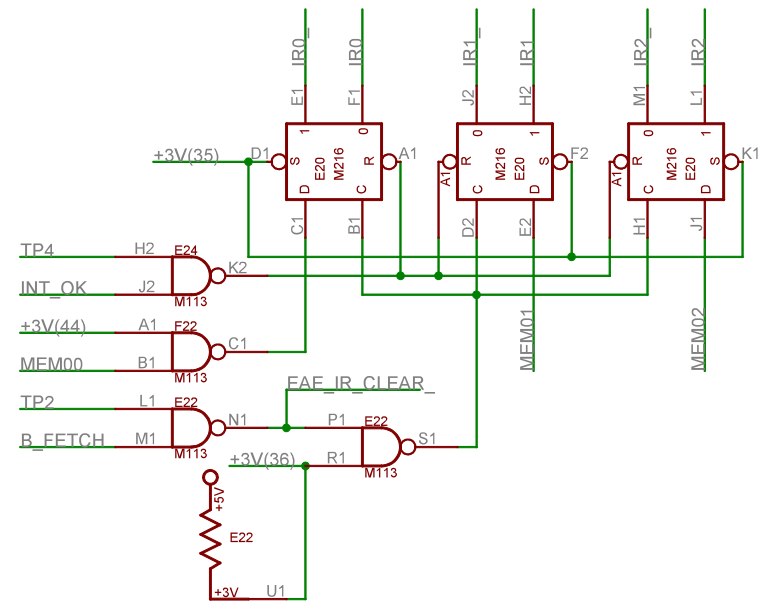
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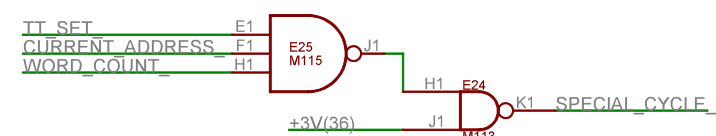
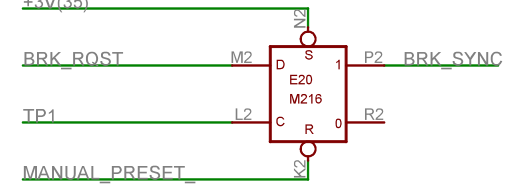
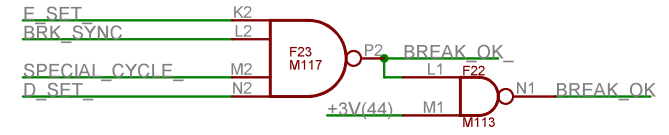
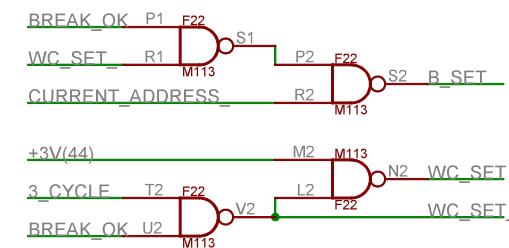
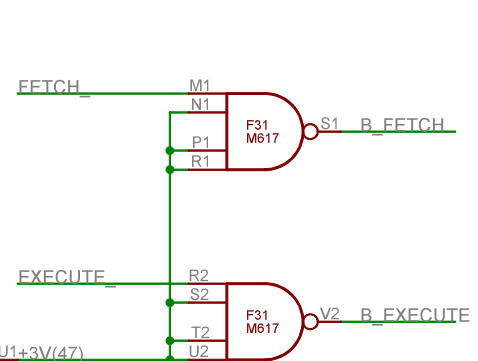
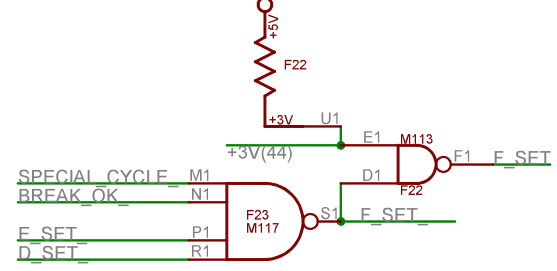
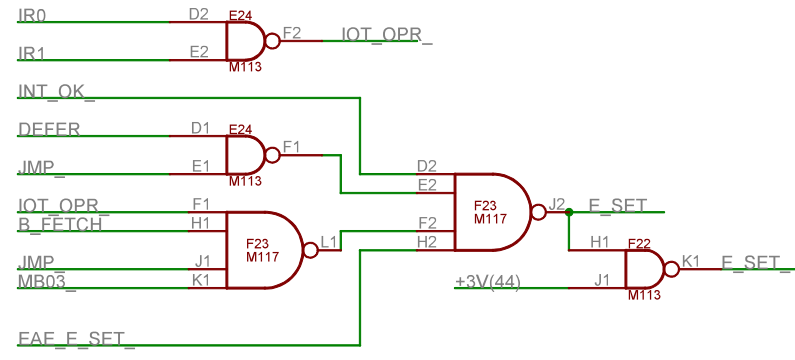
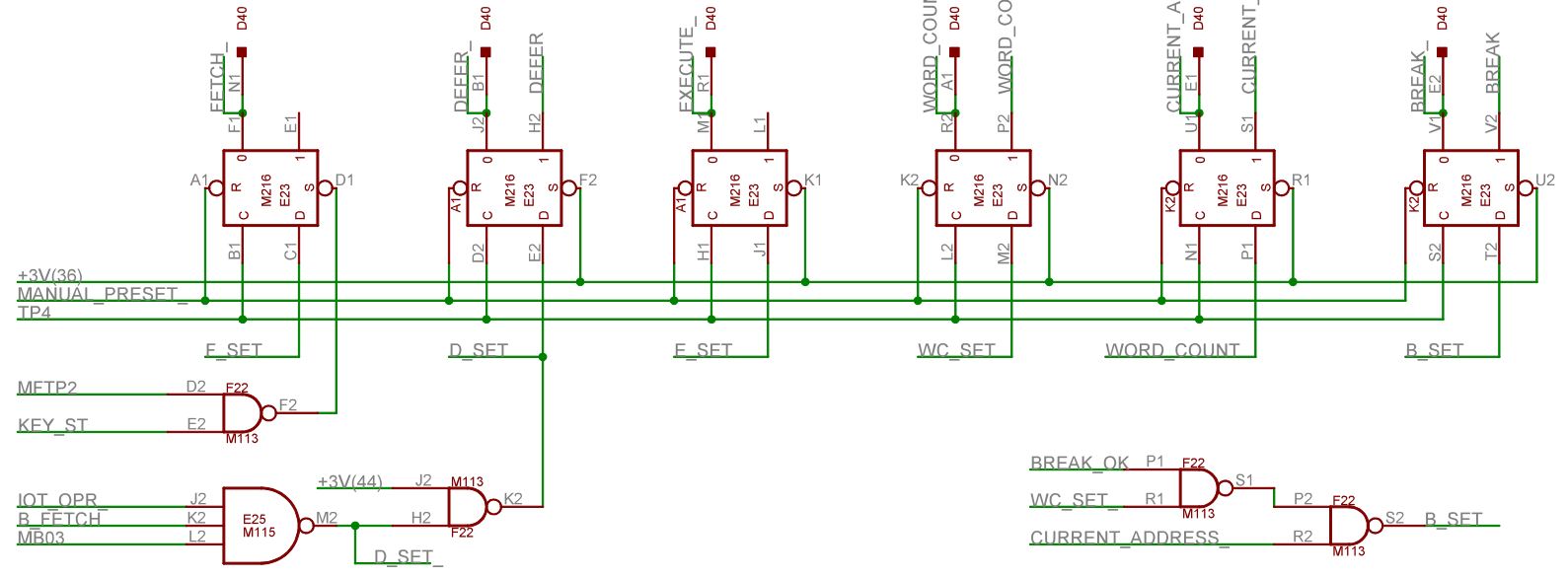
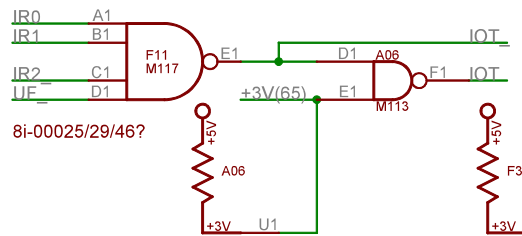


VCC  
  
 GND  


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- AND\_ M2 D40
- TAD\_ T2 D40
- ISZ\_ P1 D40
- DCA\_ R2 D40
- JMS\_ S1 D40
- IMP\_ L2 D40
- IOT\_ H2 D40
- OPR\_ D2 D40

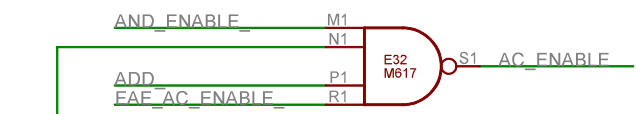
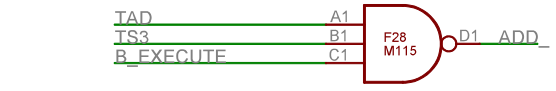
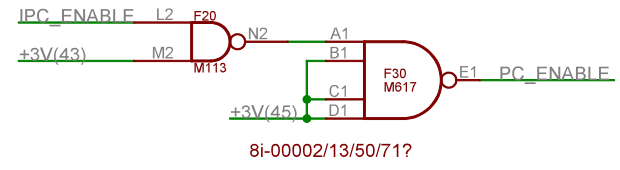
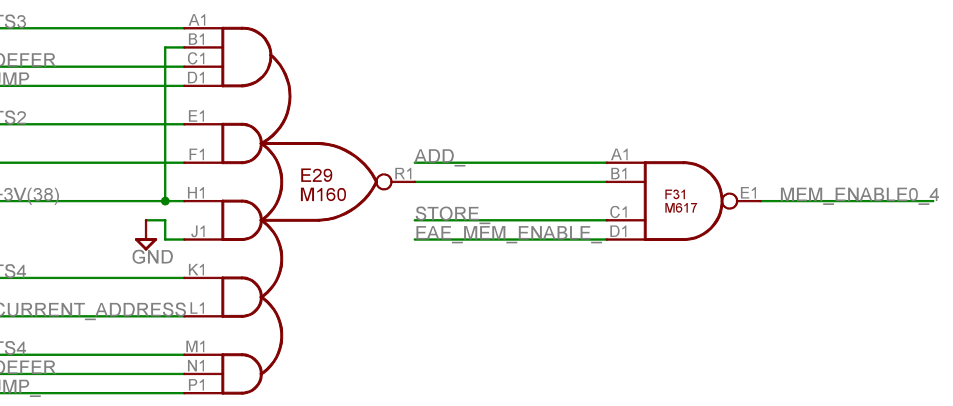
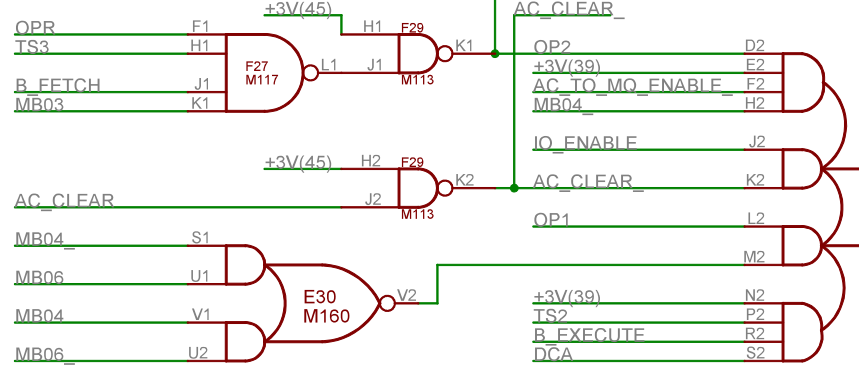
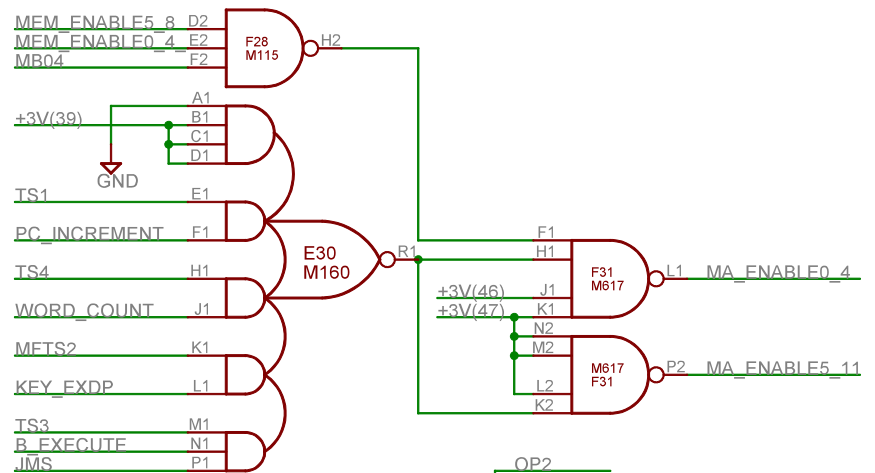
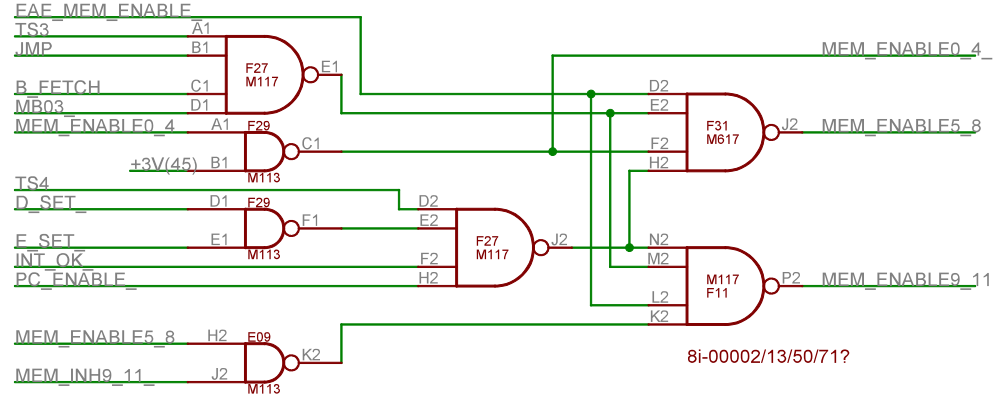
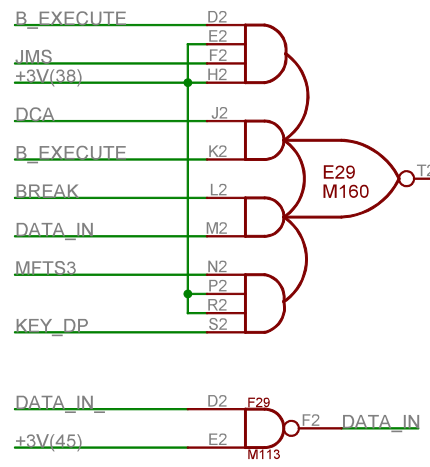
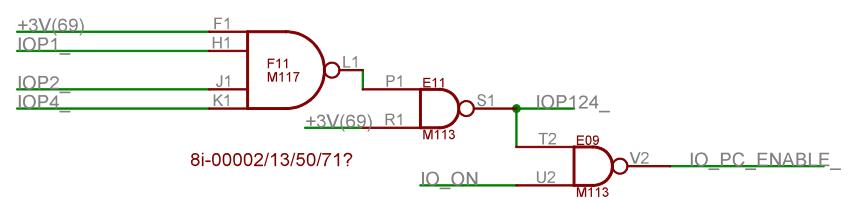
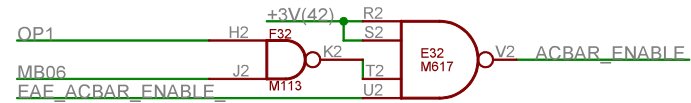
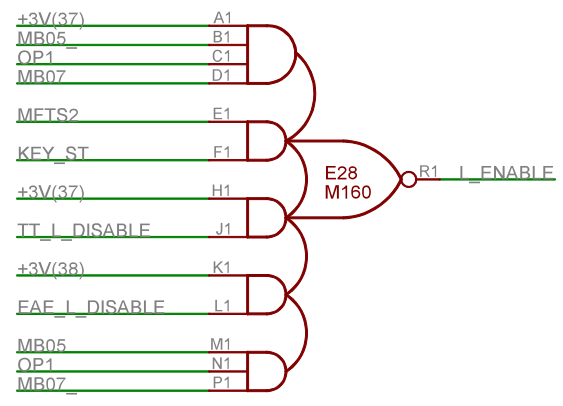
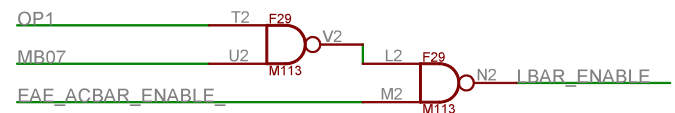
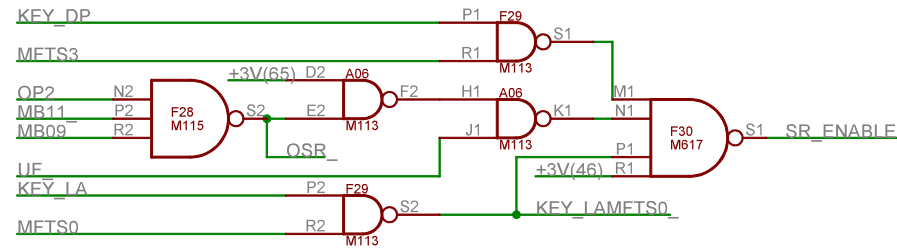
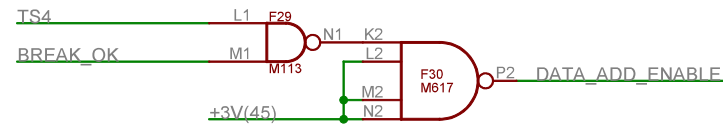
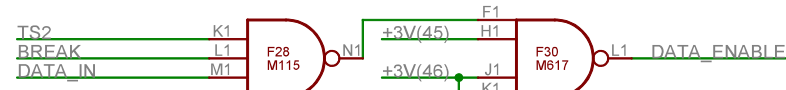
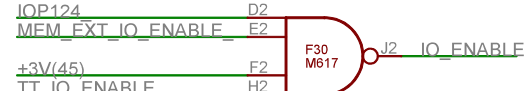
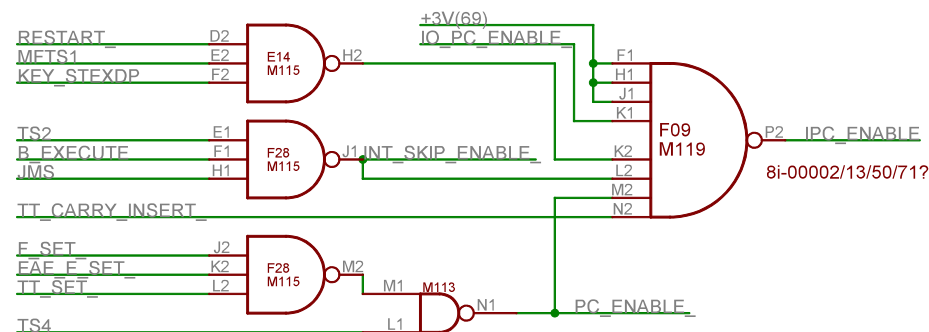


D-BS-8i-0-3 Instruction Register and Major States

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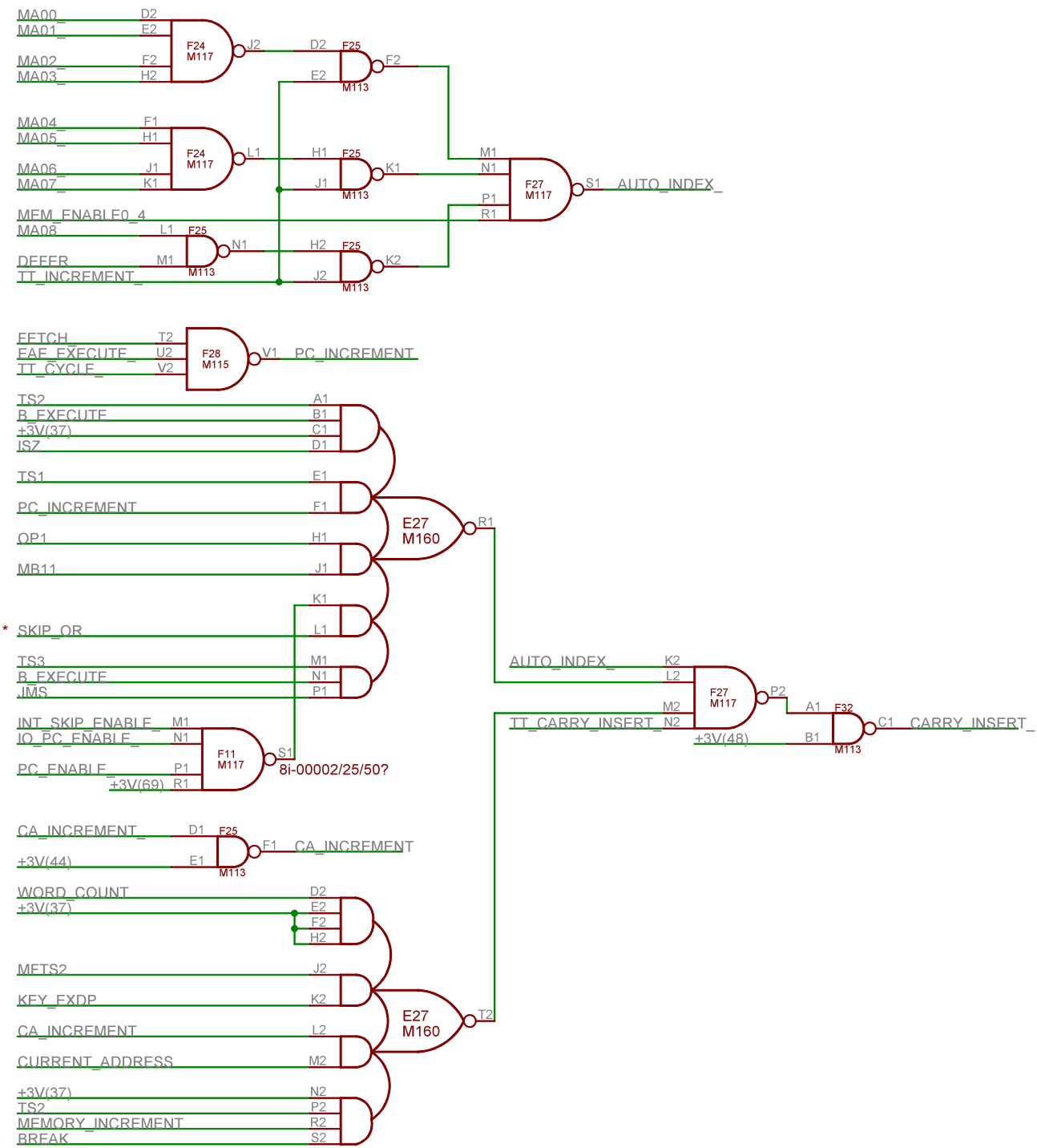




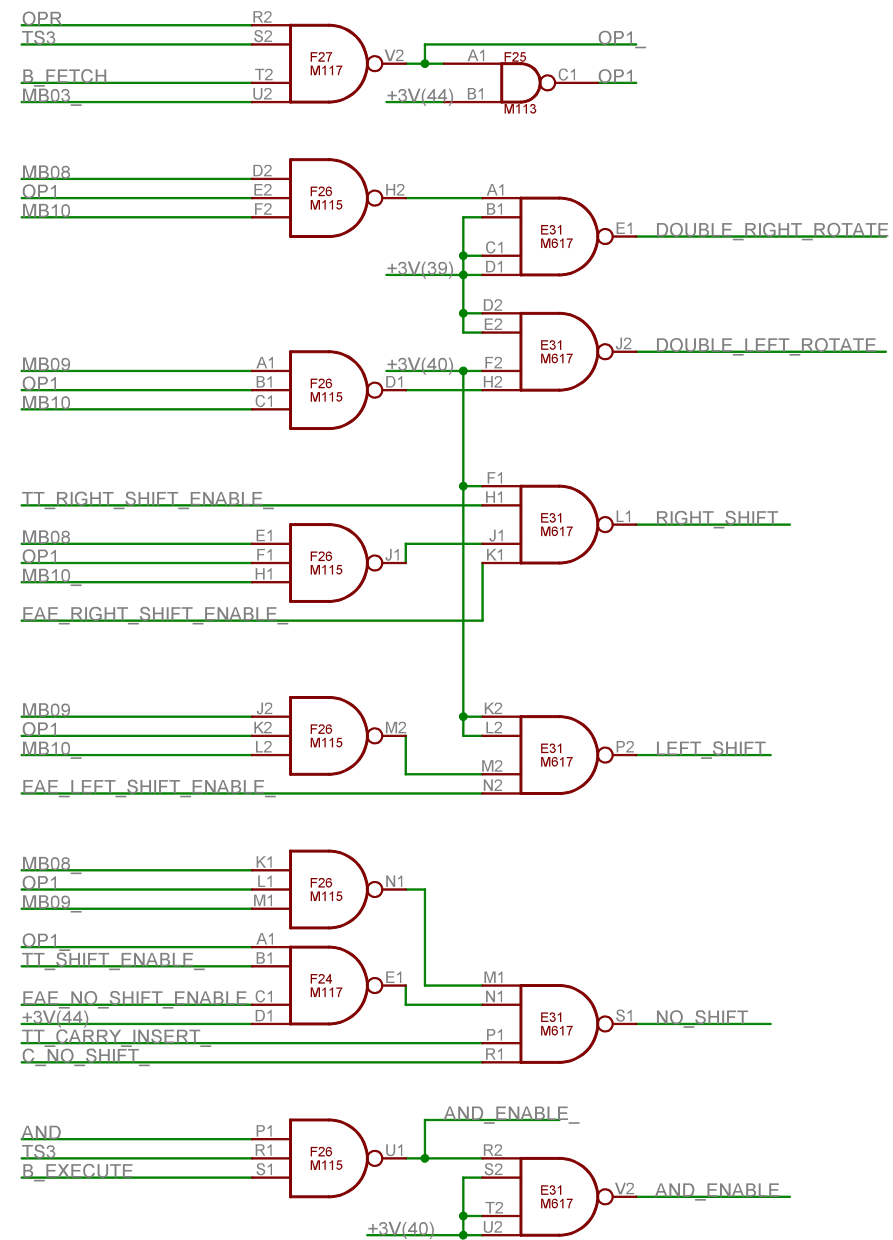


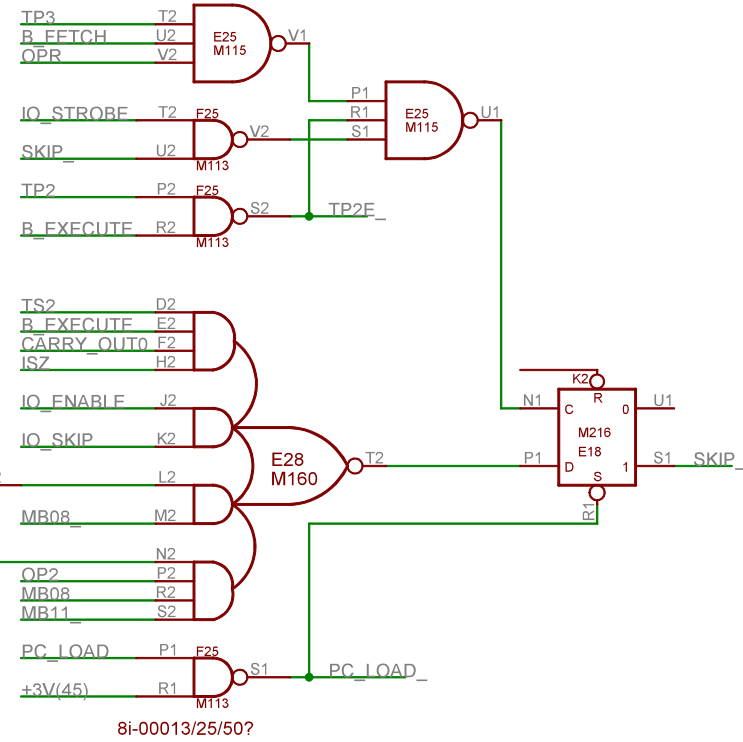
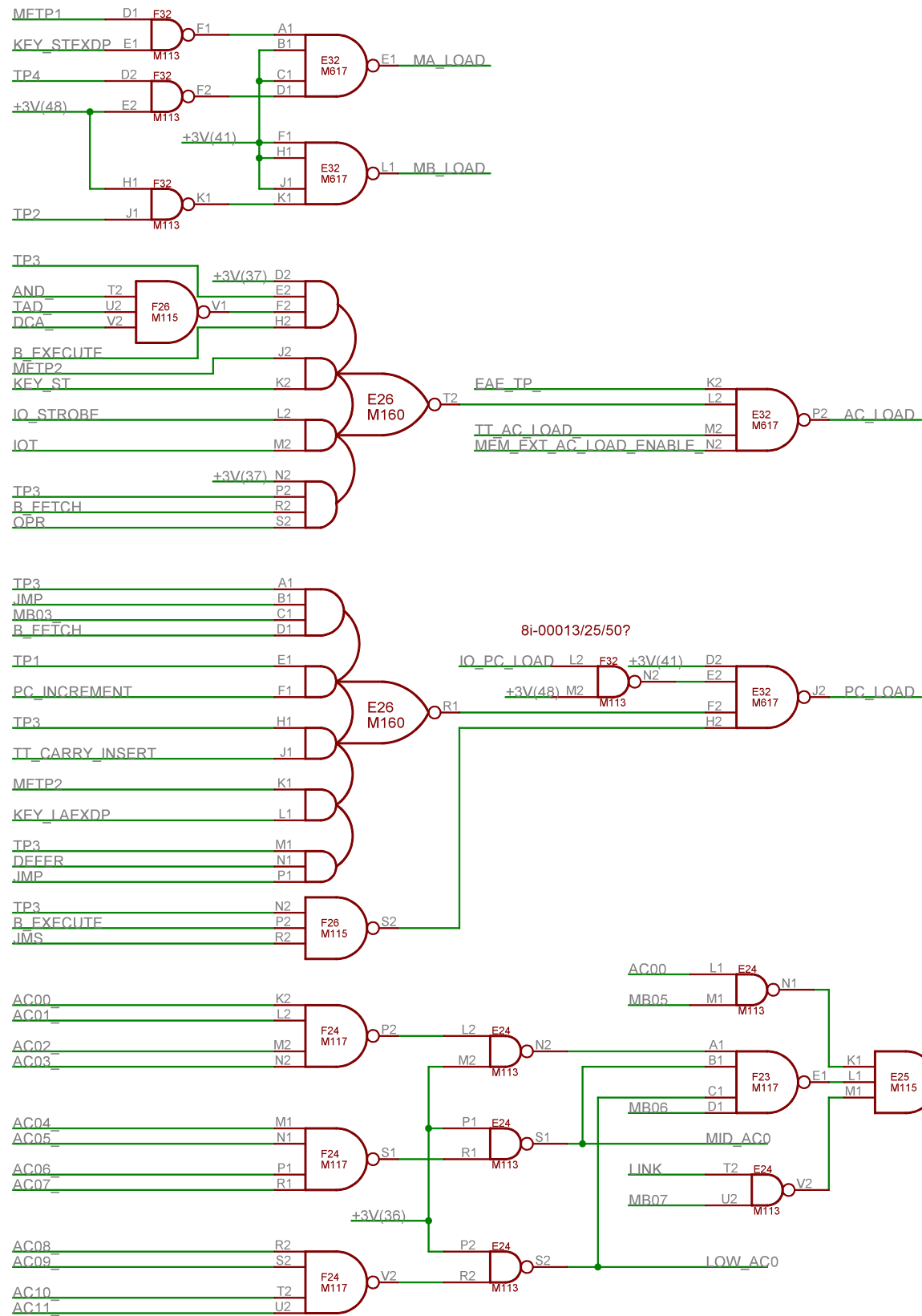
VCC  
GND

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Date: 5/11/2011 03:49:04p	Sheet: 5/40



\* If no kt8i installed, SKIP\_OR is jumpered to SKIP.  
See option jumpers (8i-0-23).

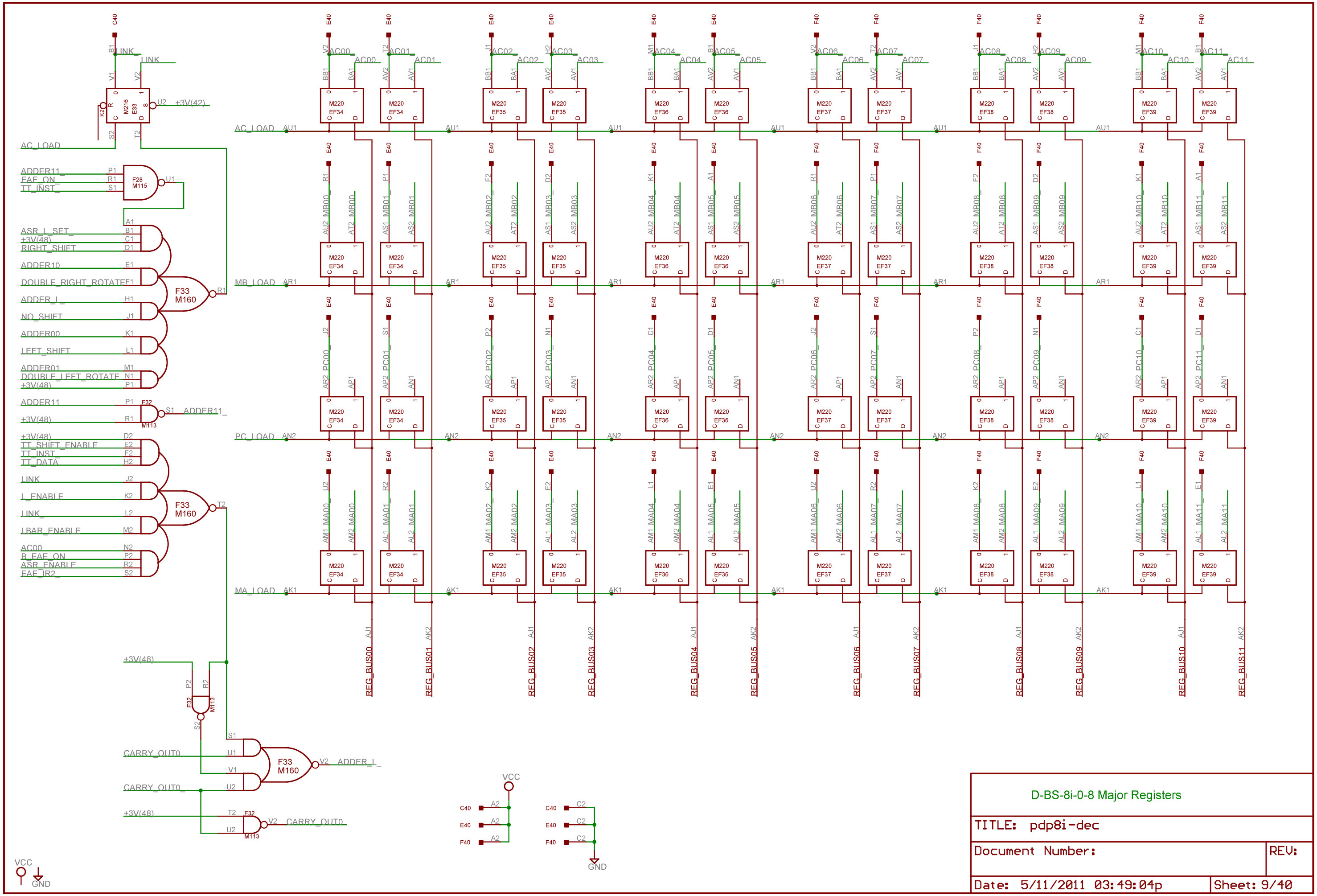




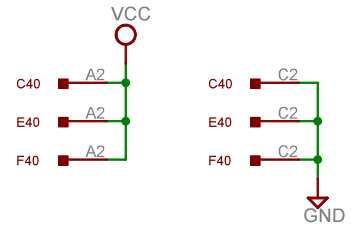
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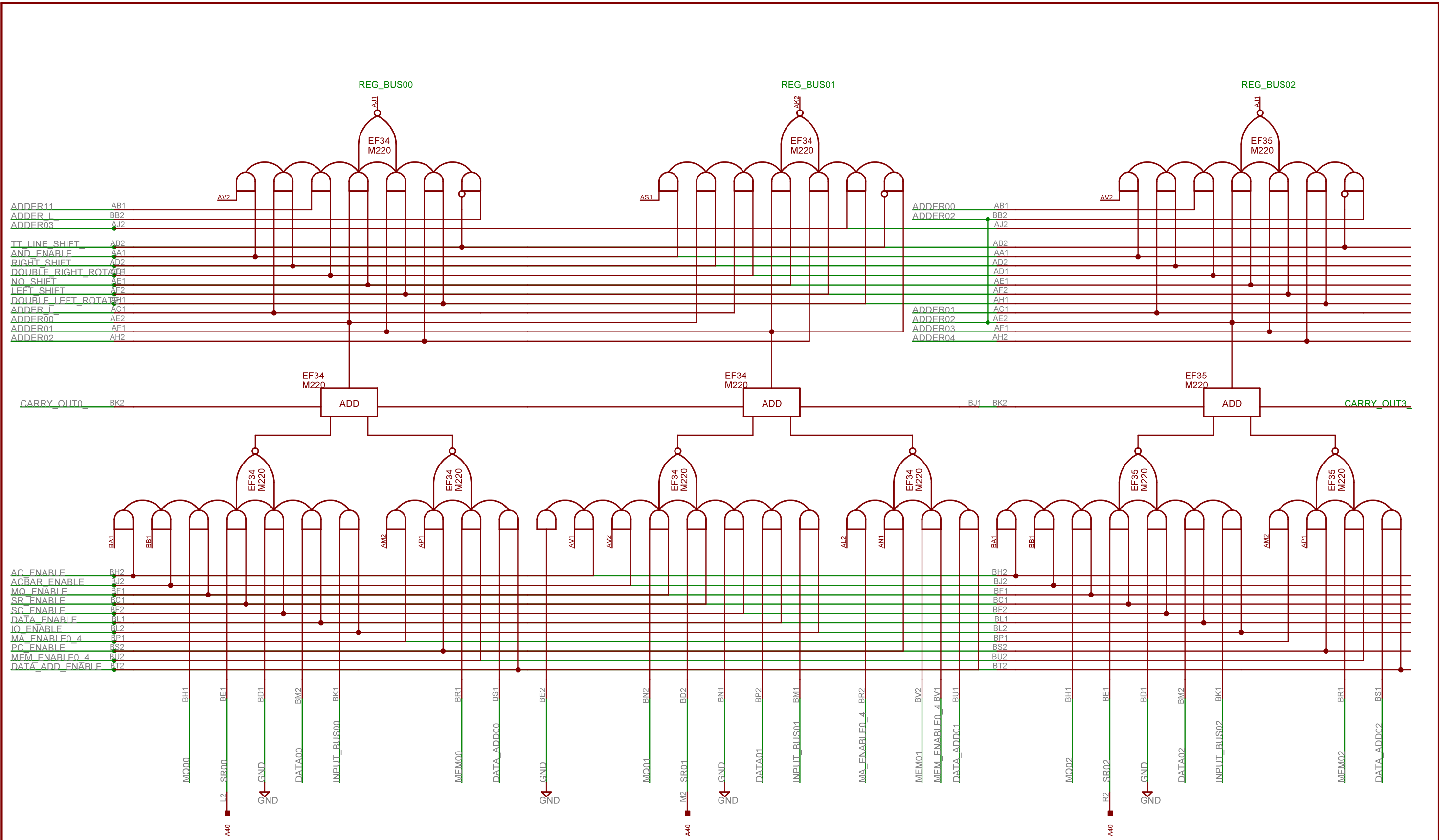






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D-BS-8i-0-9 Major Registers Gating (1/4)

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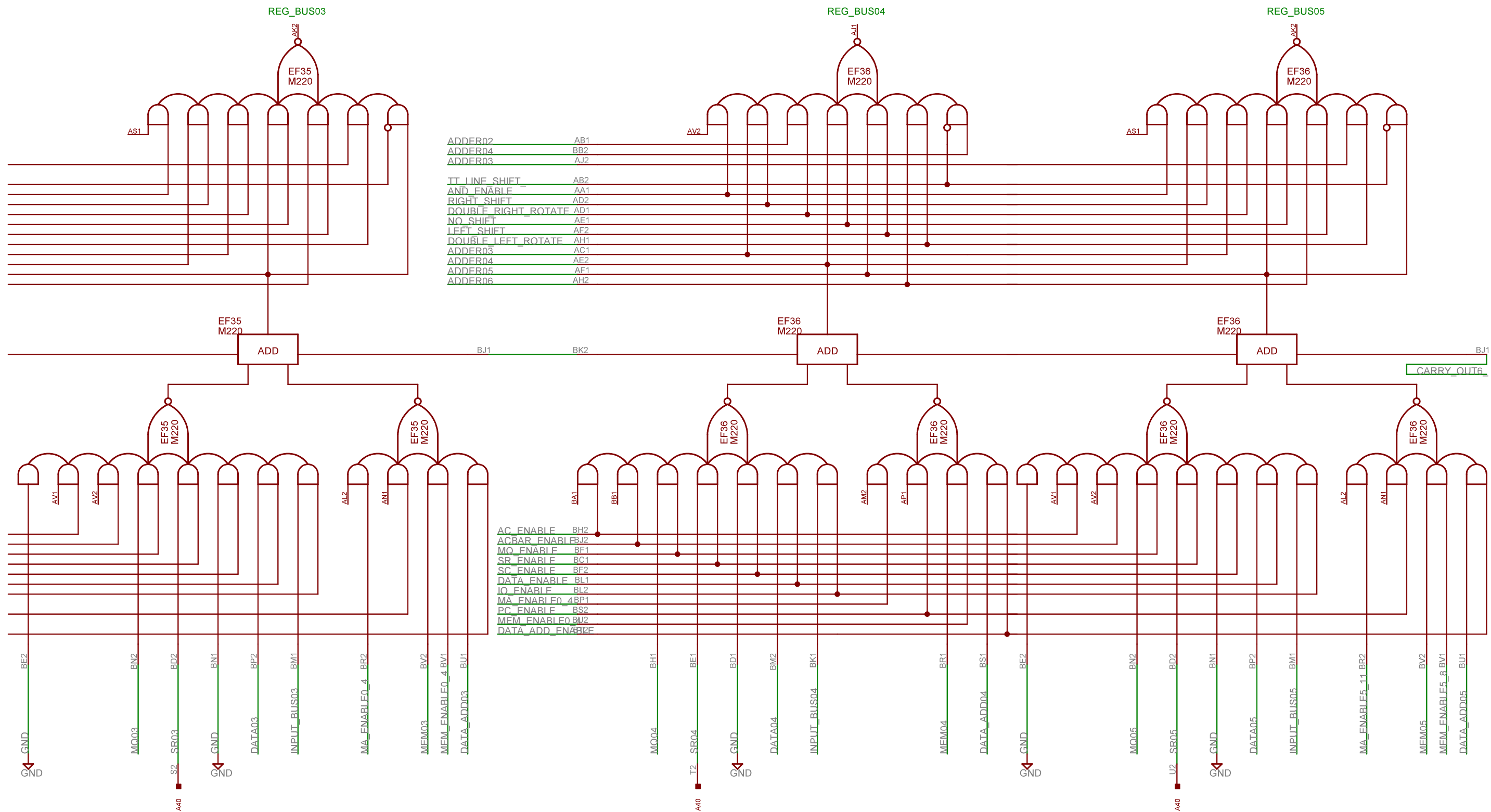
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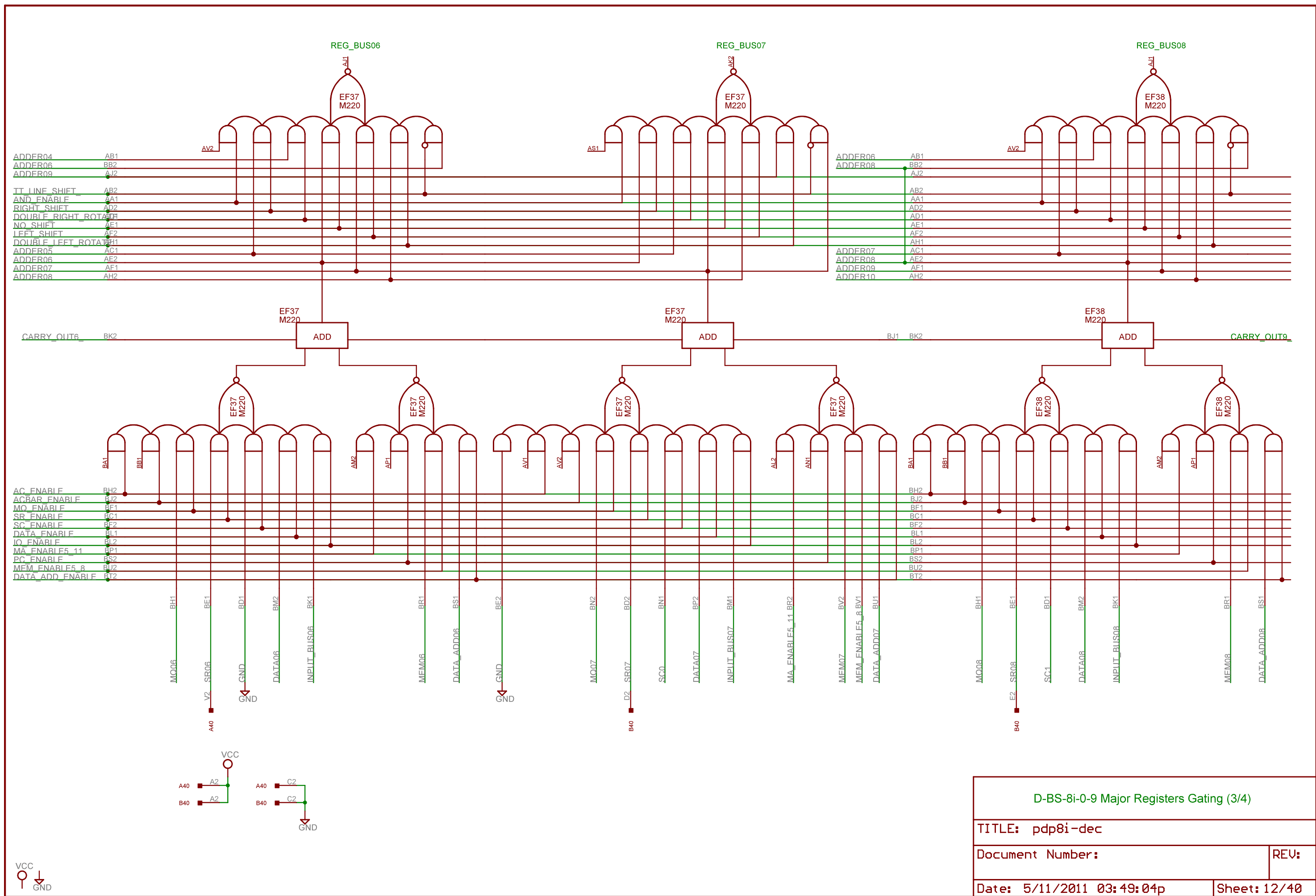




D-BS-8i-0-9 Major Registers Gating (2/4)

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D-BS-8i-0-9 Major Registers Gating (3/4)

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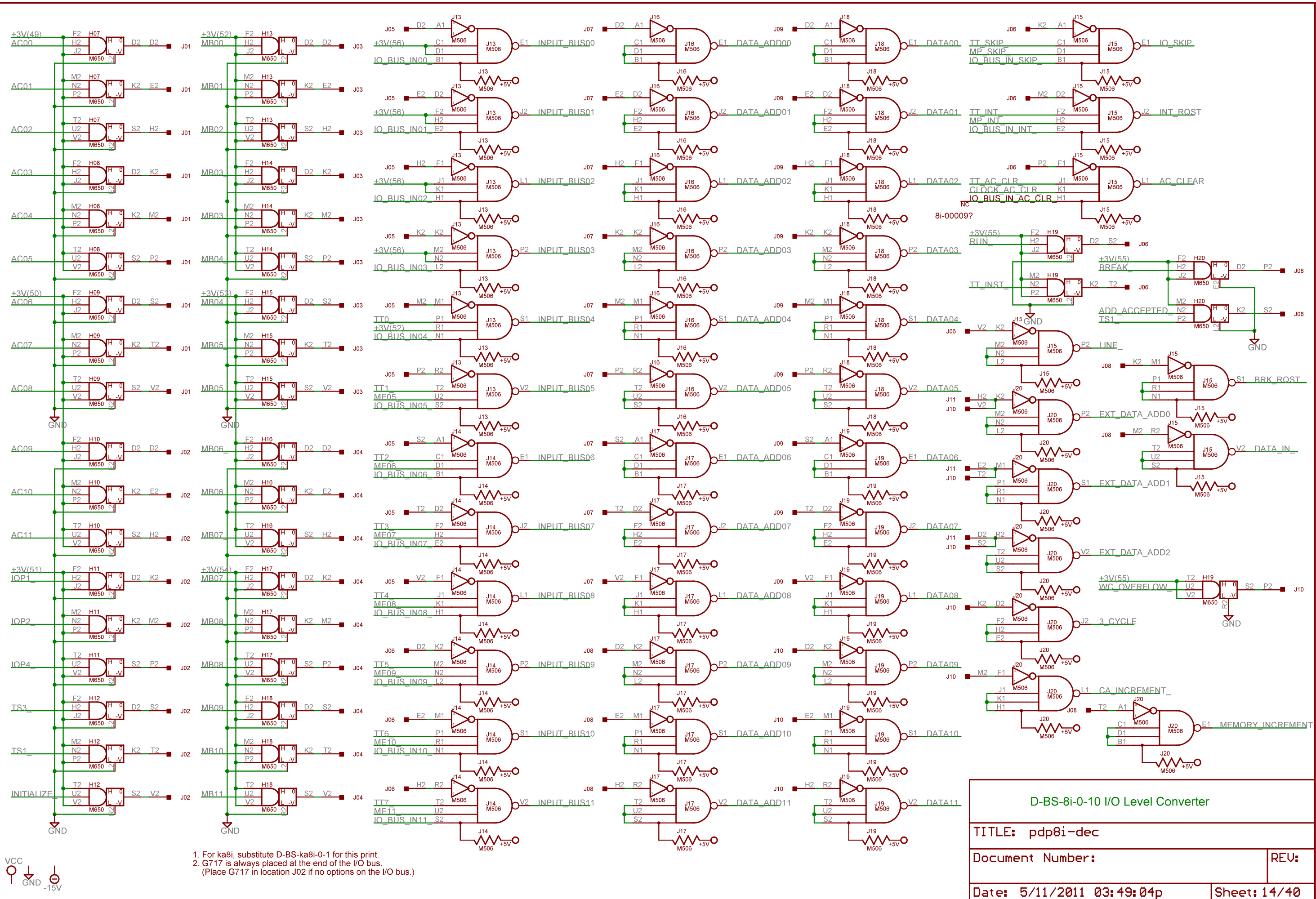
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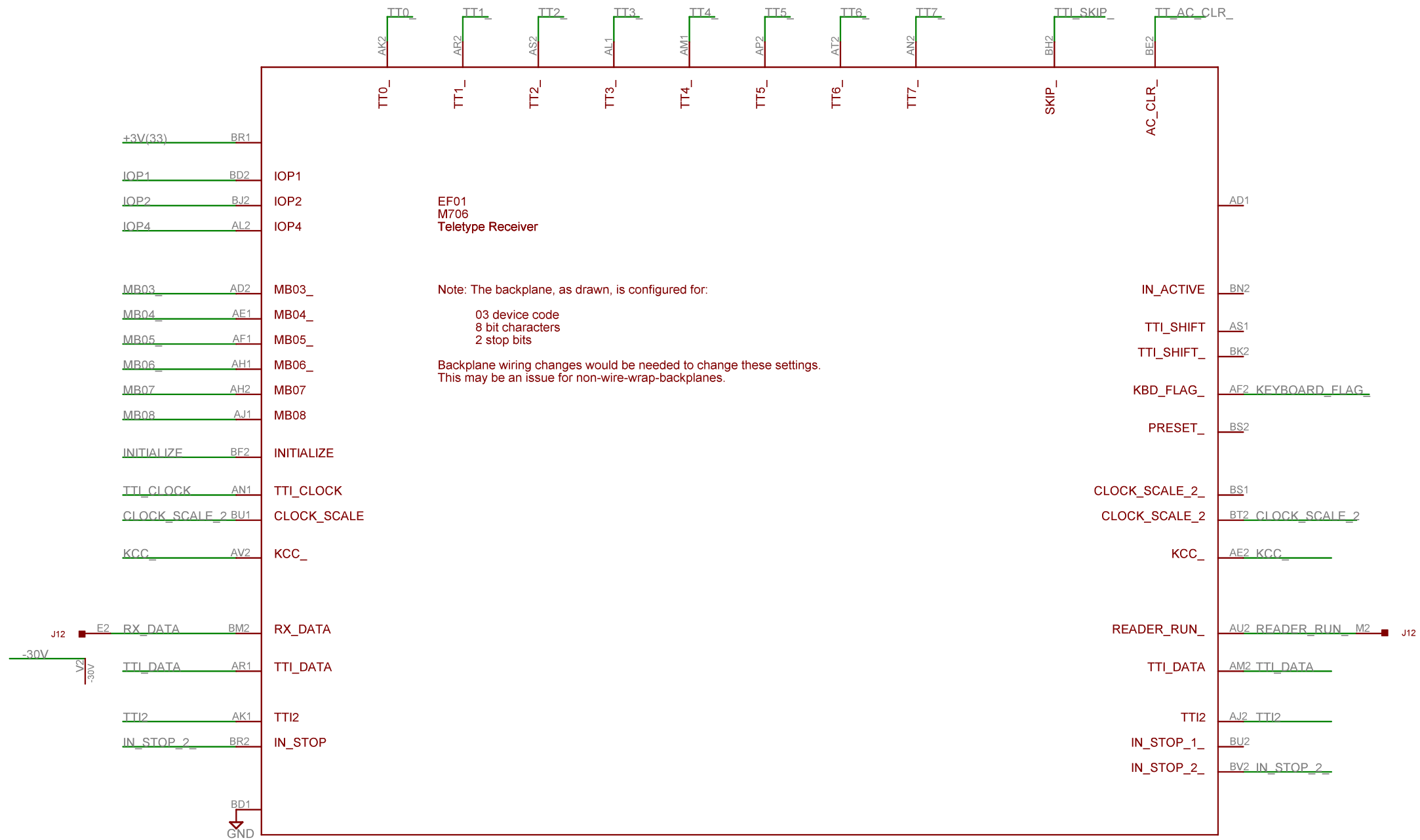
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D-BS-8i-0-11 Teletype Receivers

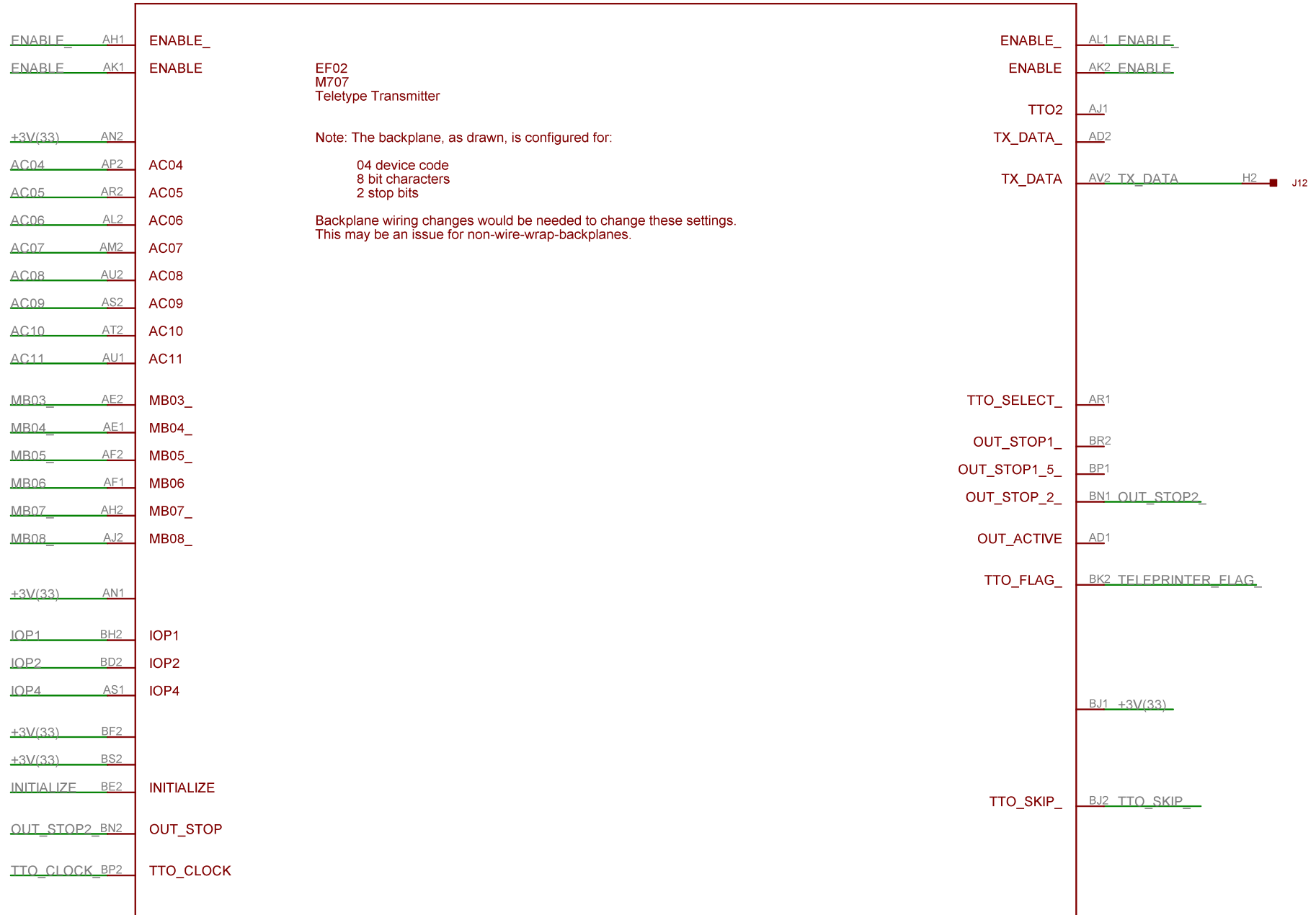
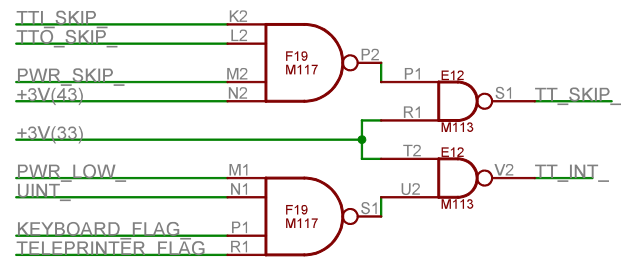
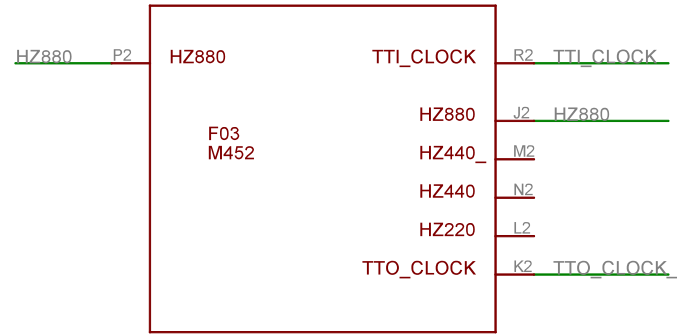
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D-BS-8i-0-12 Teletype Transmitter

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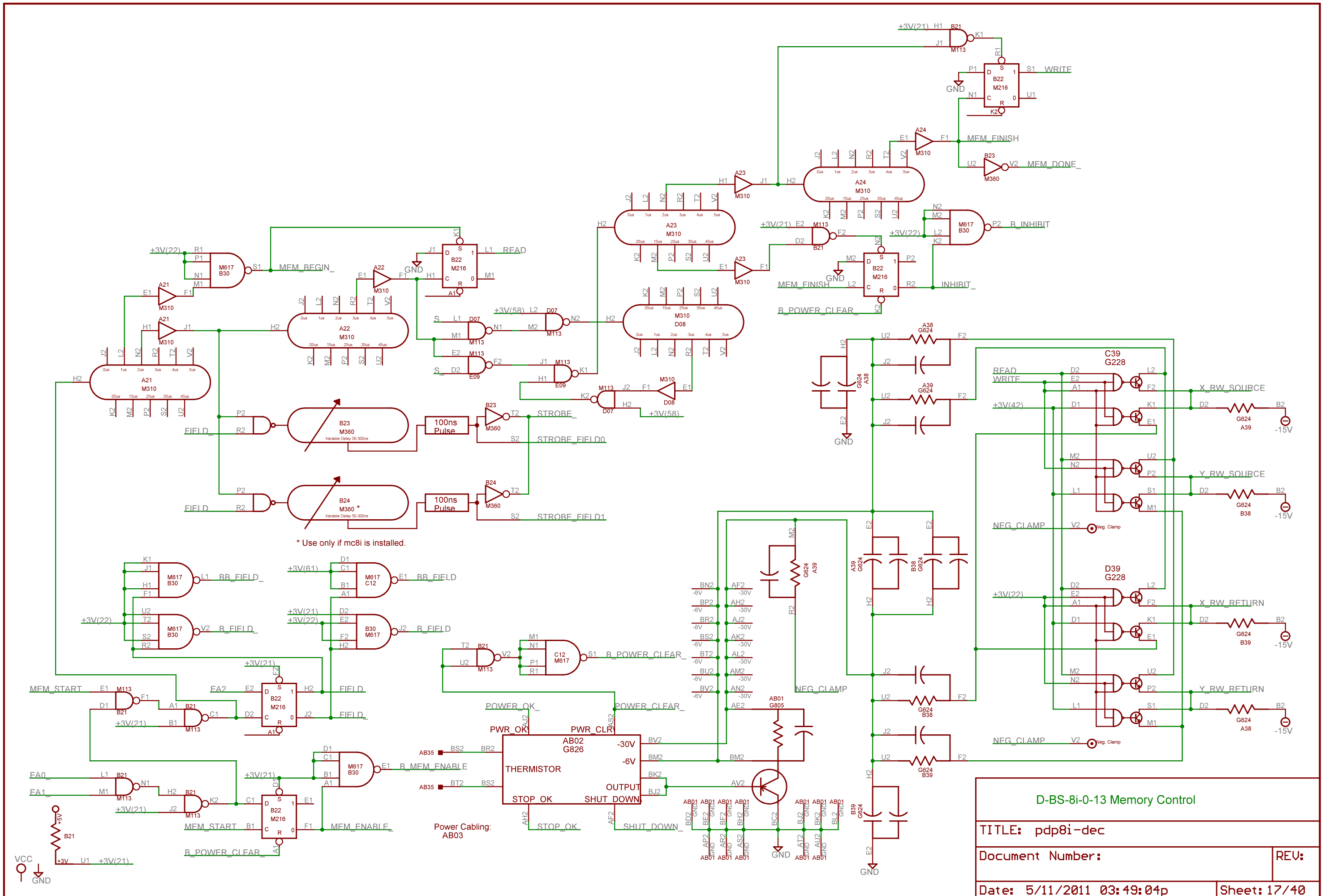
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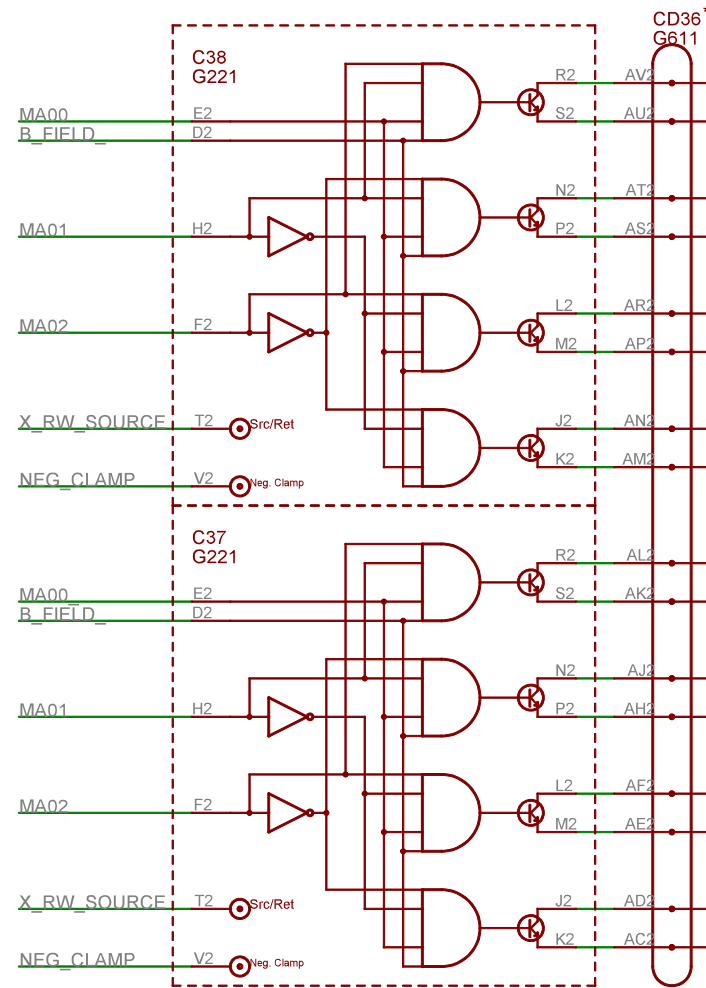
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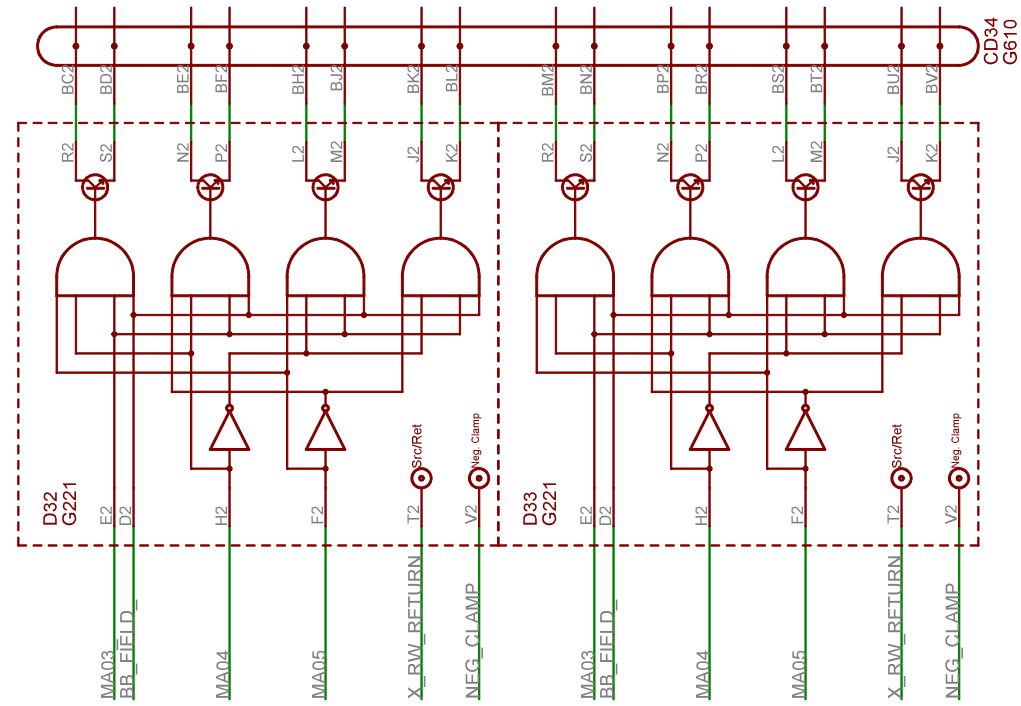
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\* G611 in CD36 is replaced with G612 for MP8i.

Core Memory:  
C35  
D35



D-BS-8i-0-15 X Axis Selection

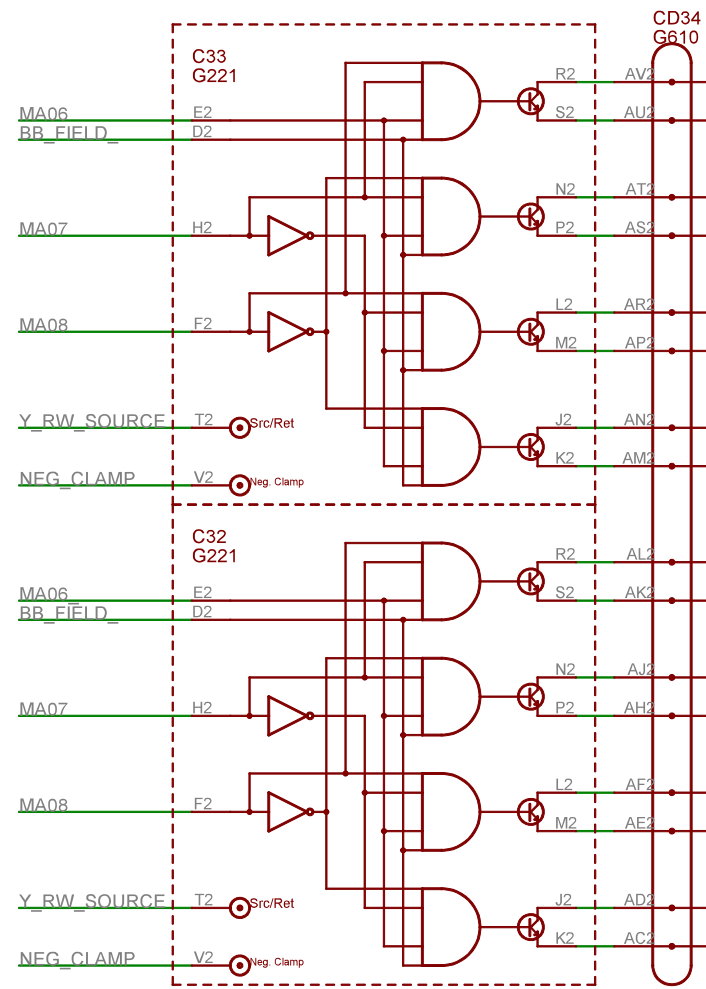
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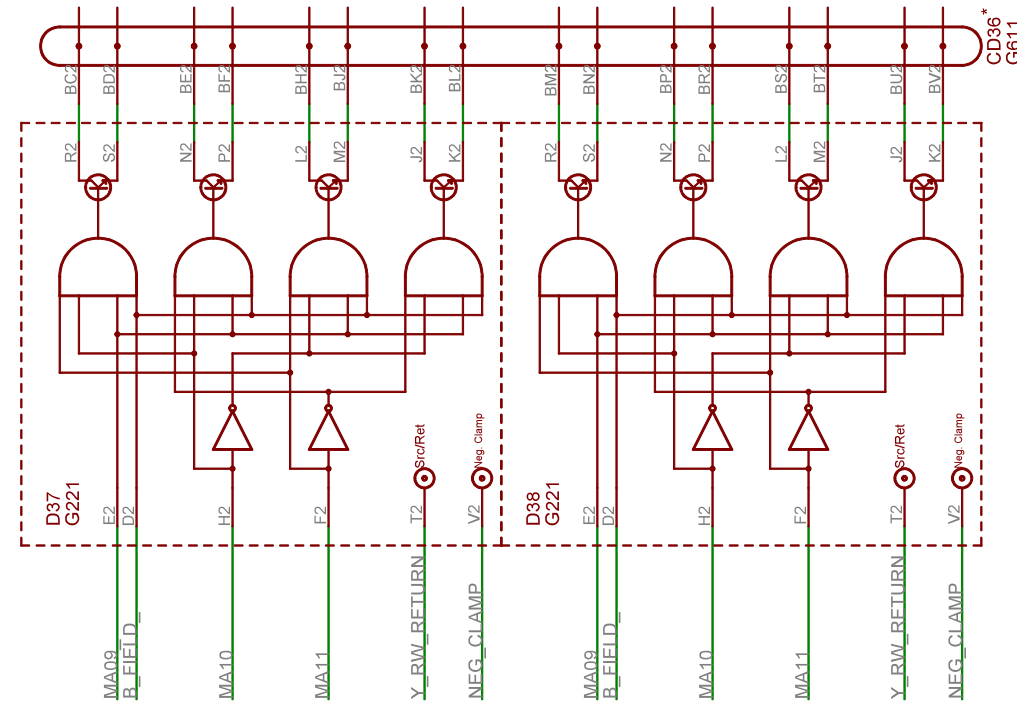
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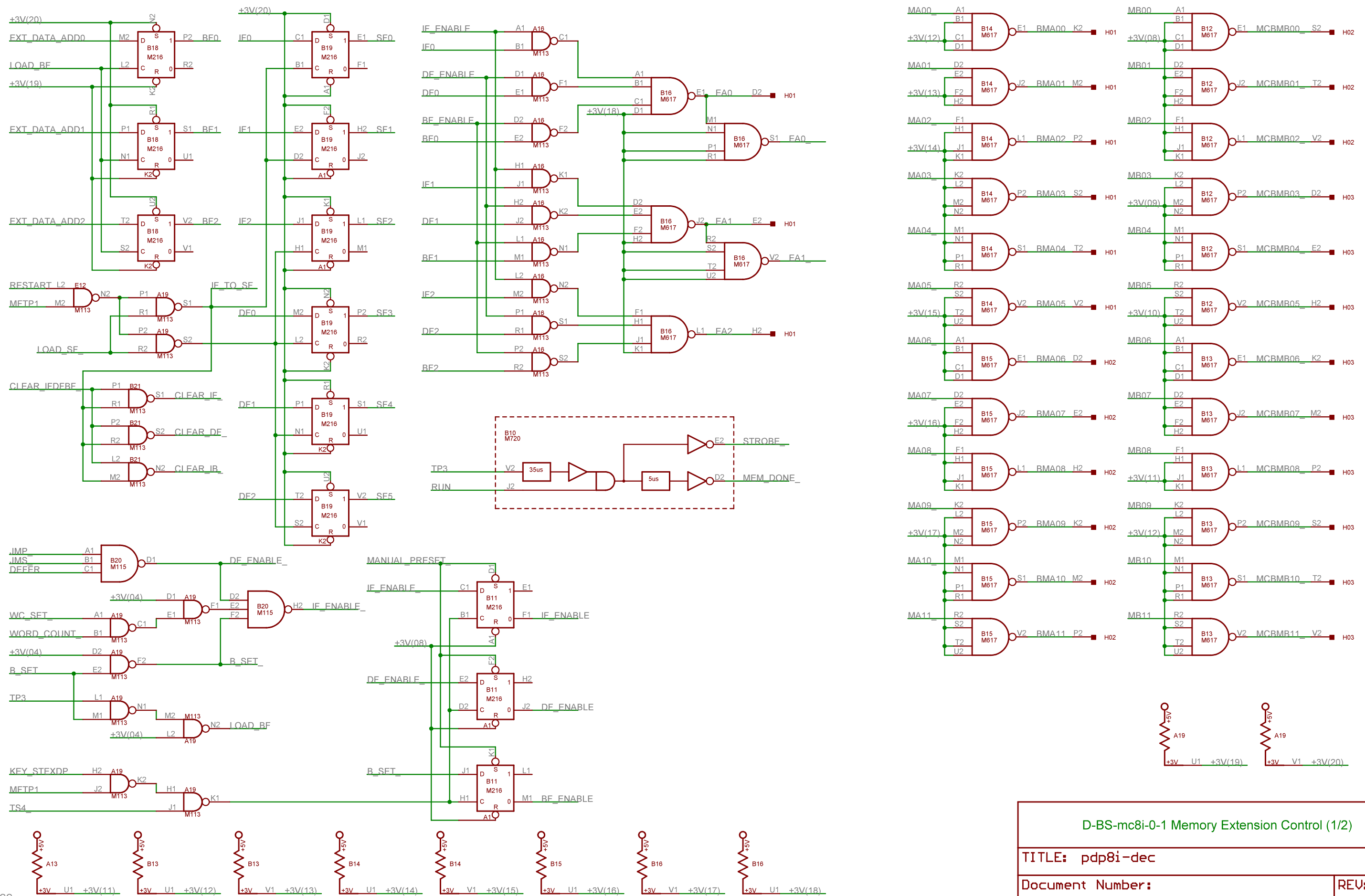
Core Memory:  
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D35



\* G611 in CD36 is replaced with G612 for MP8i.

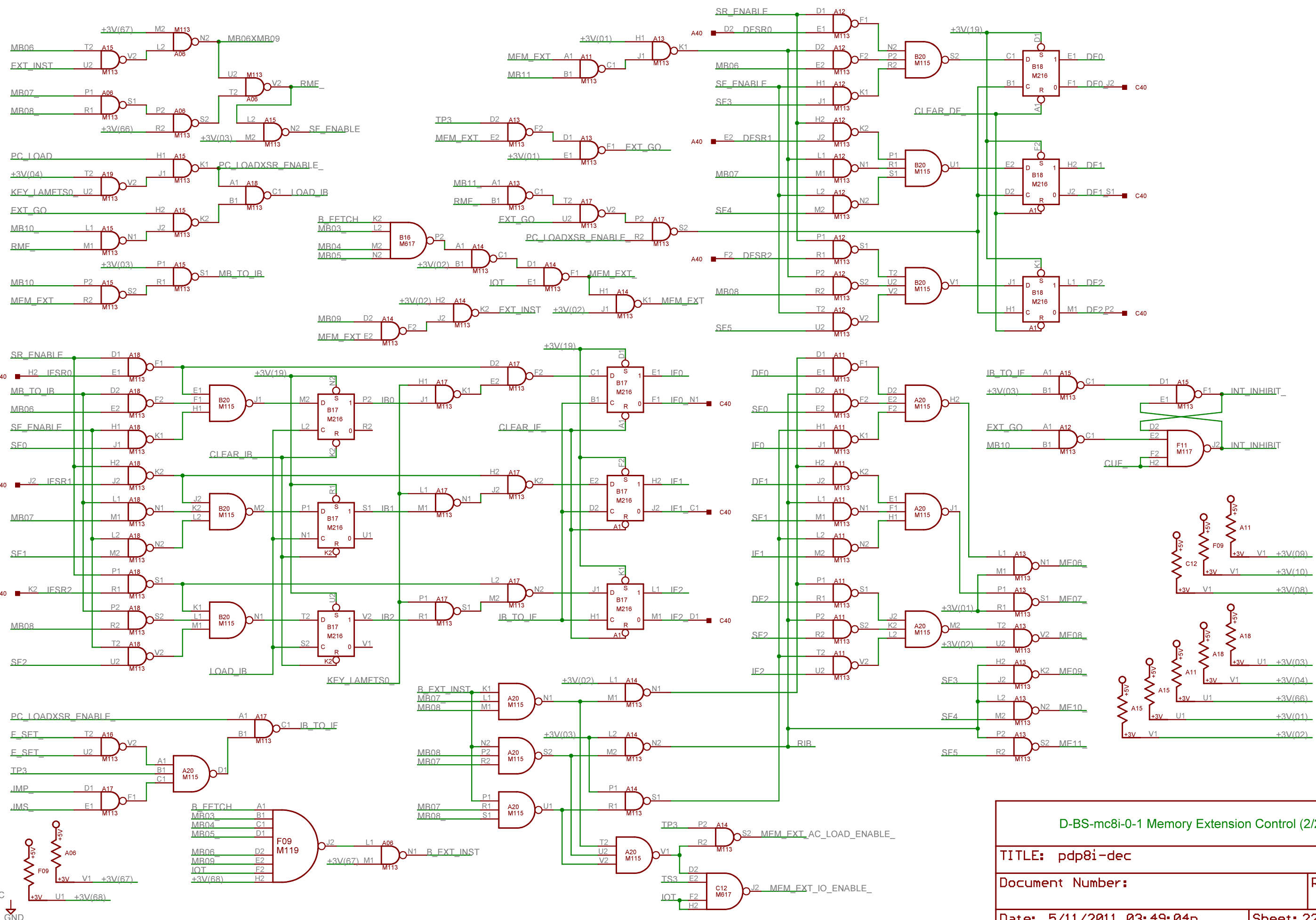


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D-BS-mc8i-0-1 Memory Extension Control (1/2)

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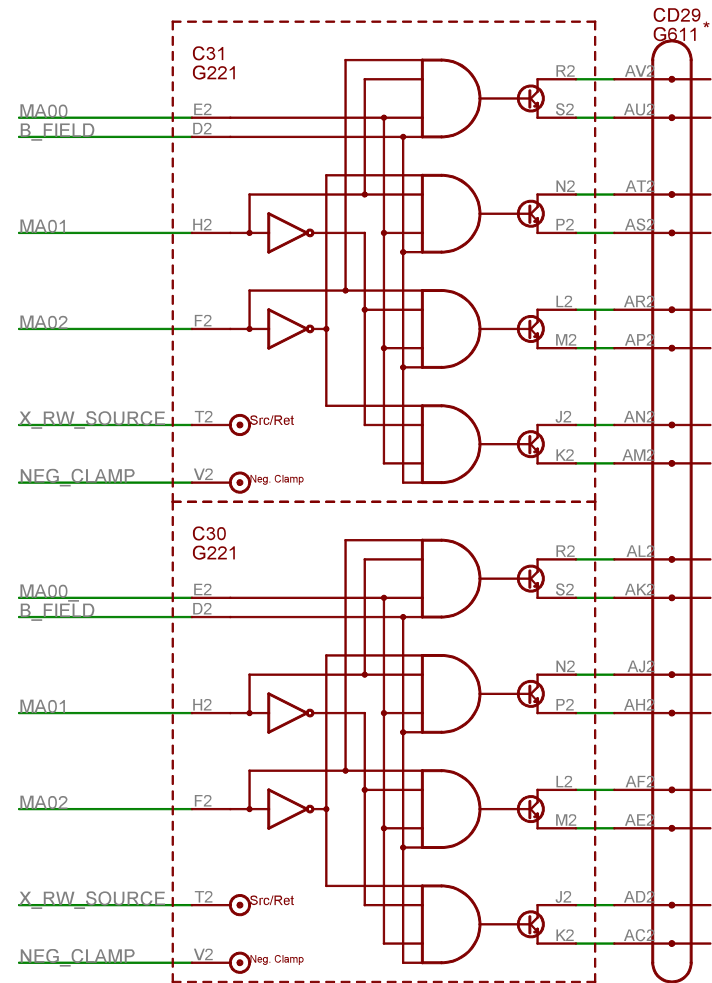


D-BS-mc8i-0-1 Memory Extension Control (2/2)

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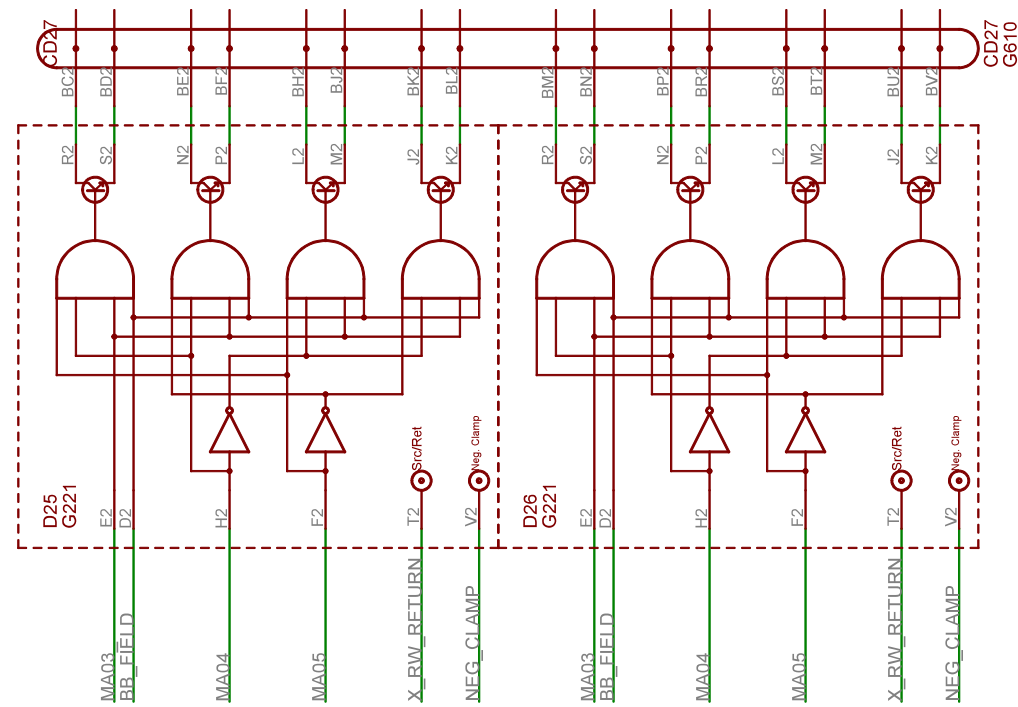






\* G611 in CD29 is replaced with G612 for MP8i.

Core Memory:  
C28  
D28



VCC  
GND

D-BS-mc8i-0-3 X Axis Selection

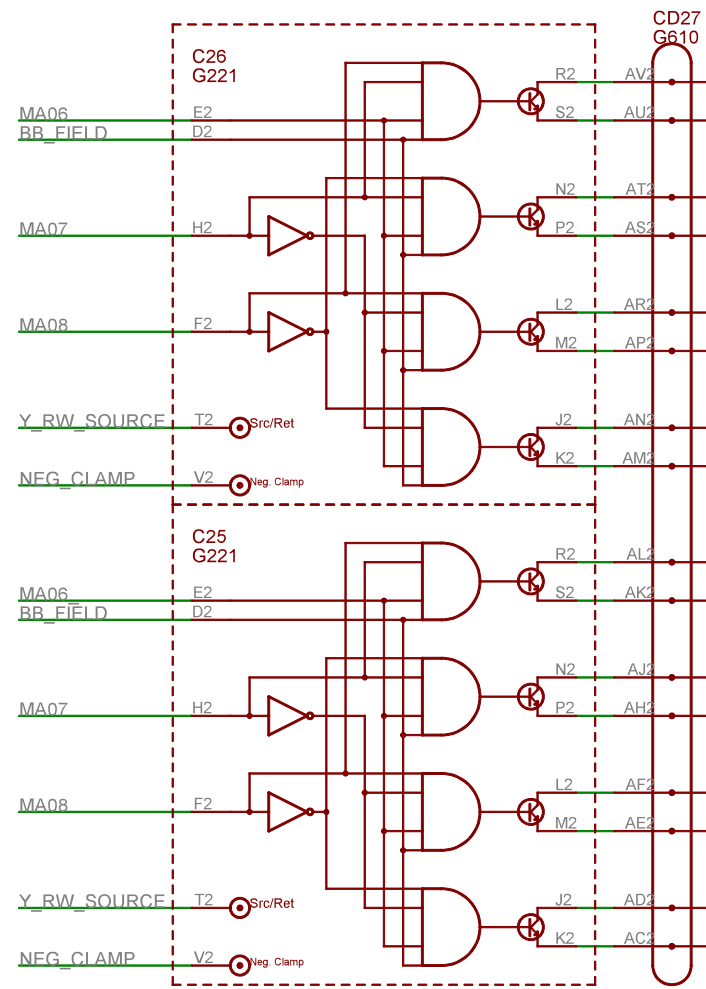
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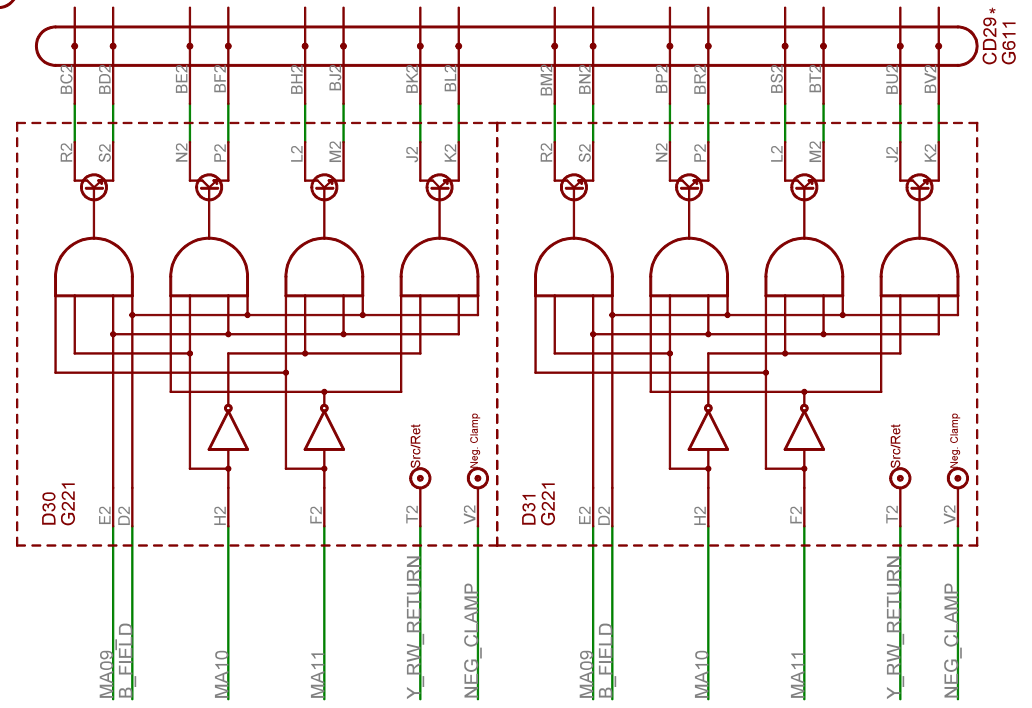
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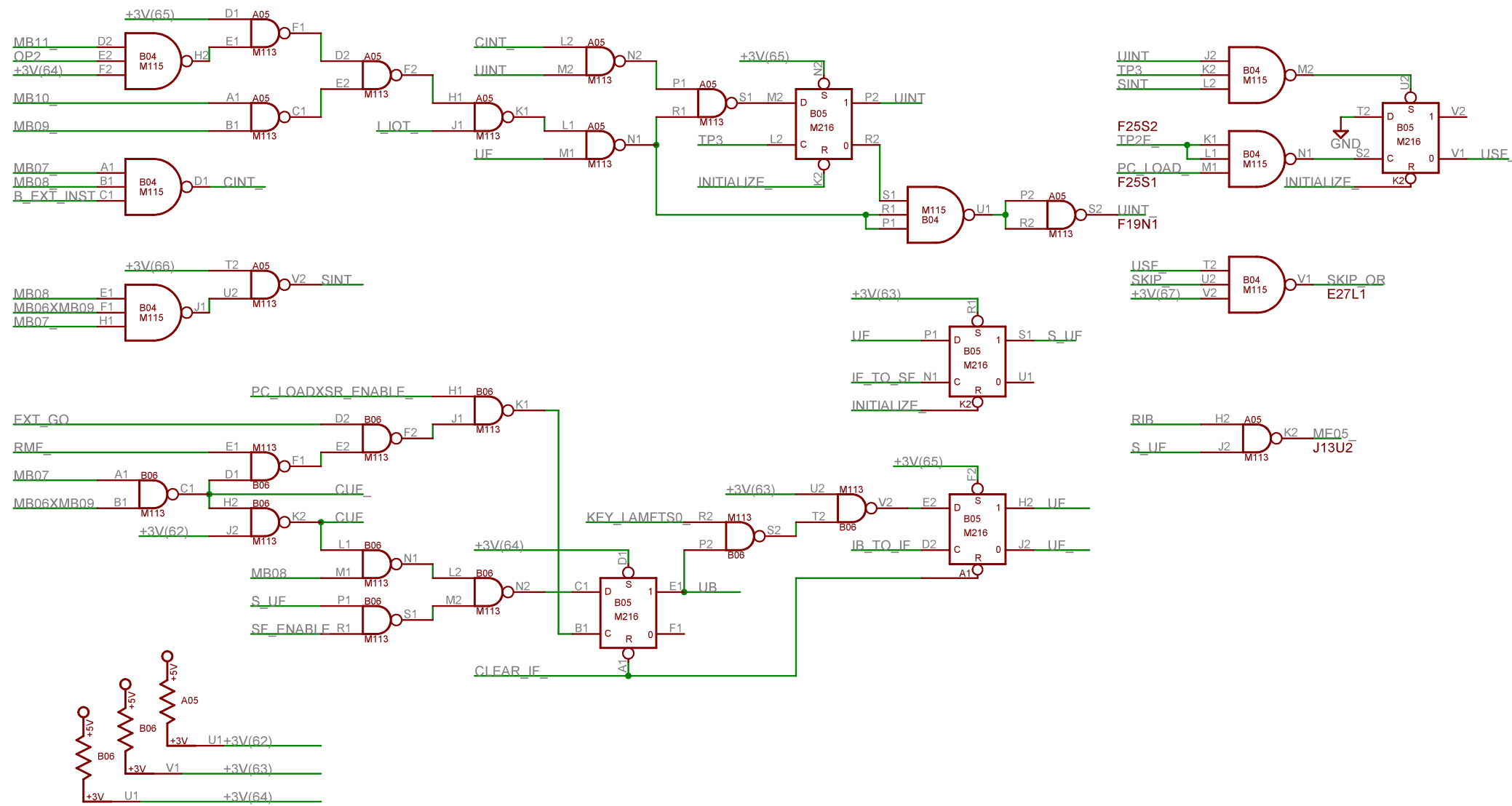
Core Memory:  
C28  
D28



\* G611 in CD29 is replaced with G612 for MP8i.



D-BS-mc8i-0-4 Y Axis Selection	
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NOTE:

PIN	PRINT	LOCATION
J13U2	8i-0-10	C-6
F19N1	8i-0-12	A-6
E27L1	8i-0-5	D-3
F25S2	8i-0-6	B-4
F25S1	8i-0-6	D-2

(Locations refer to DEC drawings.)



D-BS-kt8i-0-1 Time-share Option

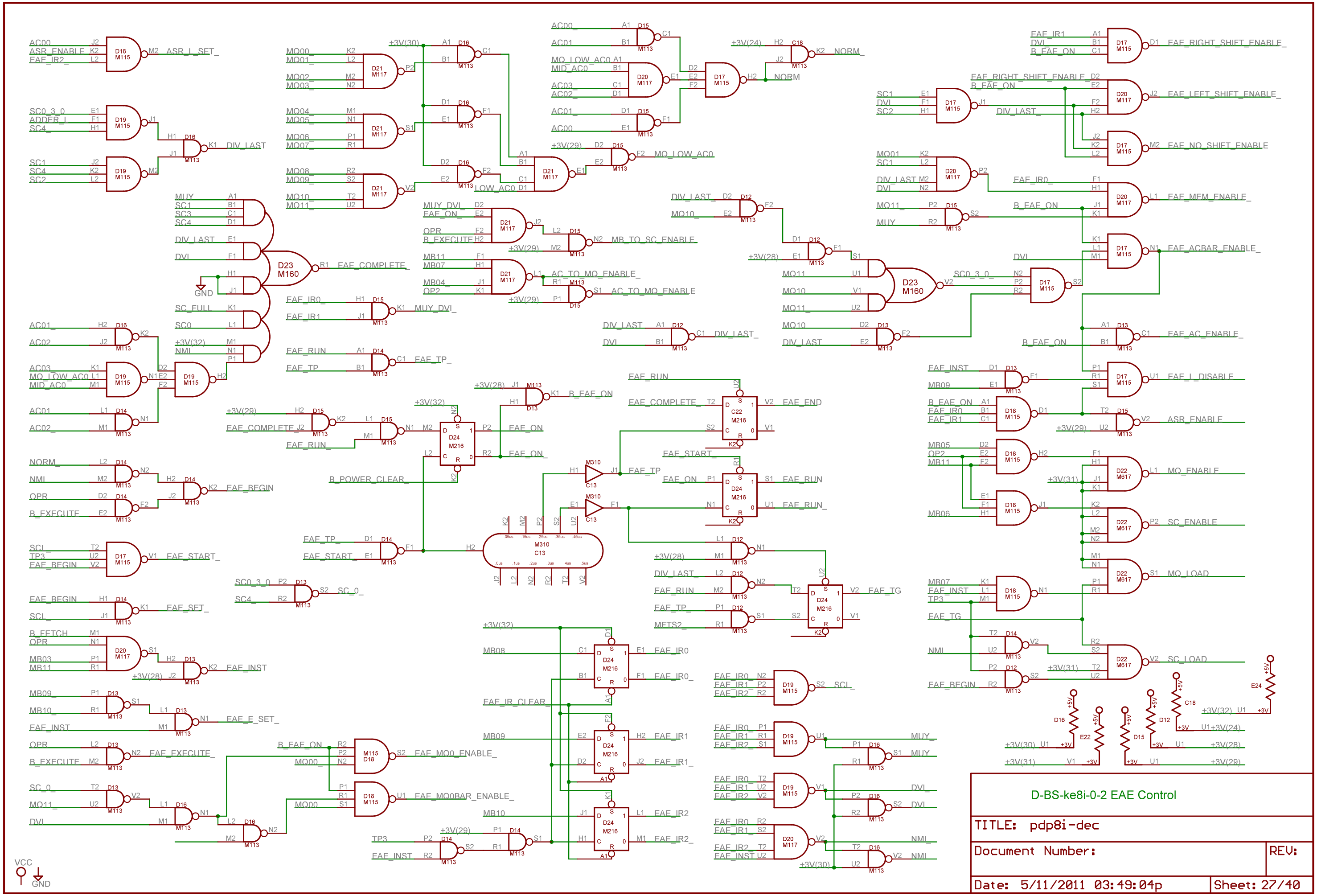
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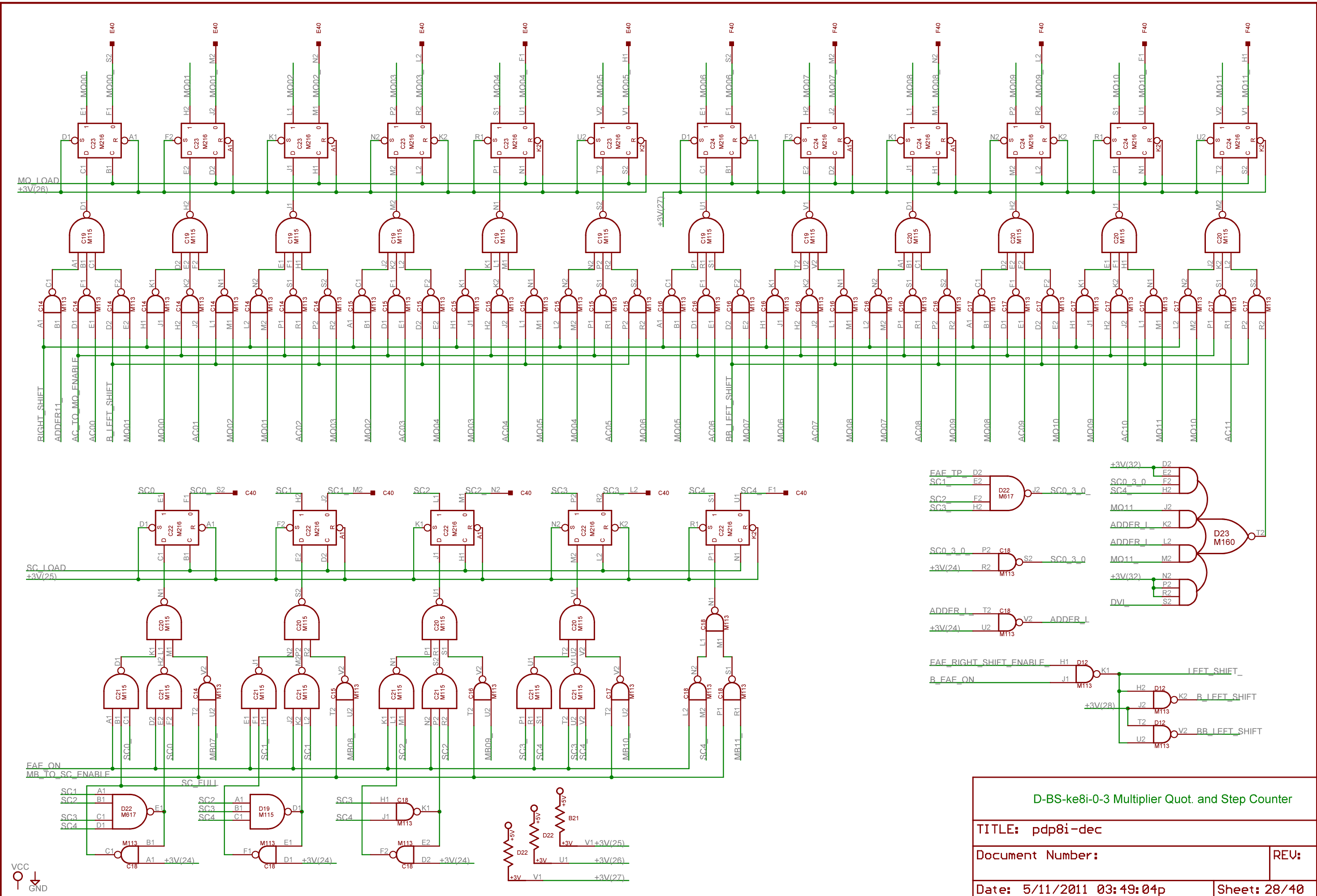
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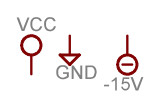
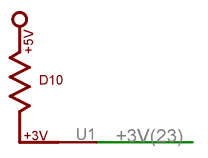
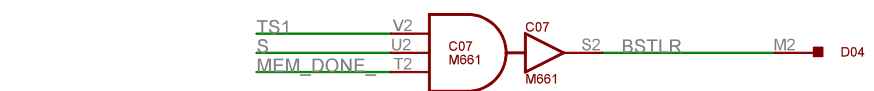
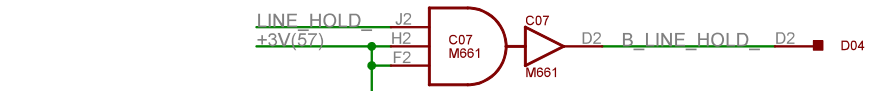
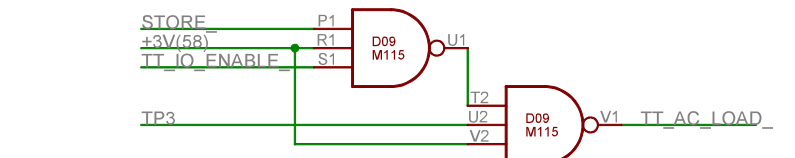
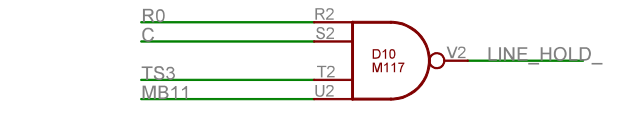
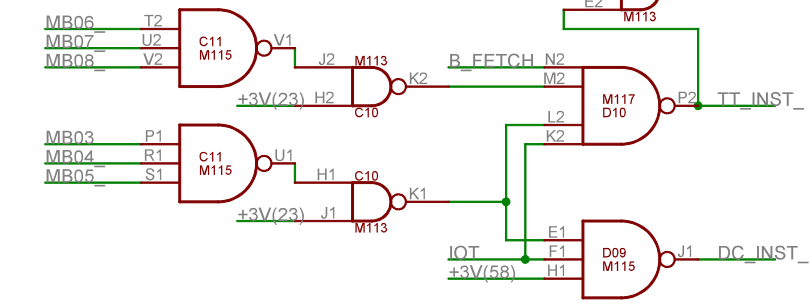
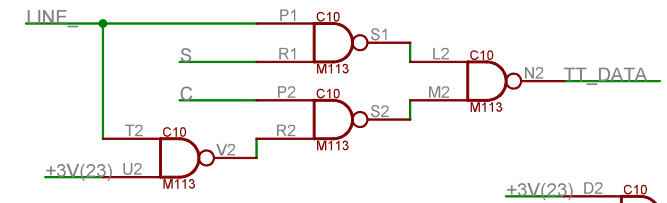
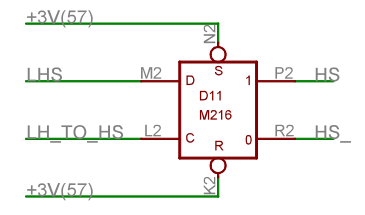
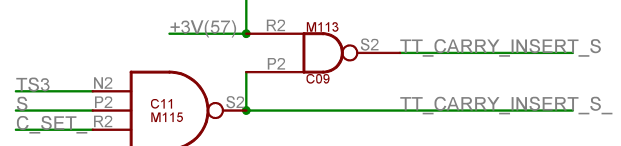
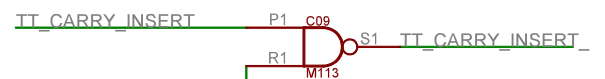
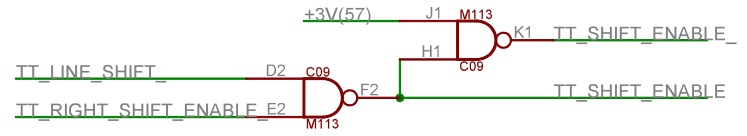
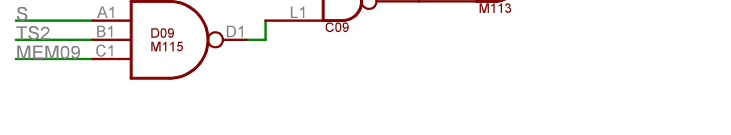
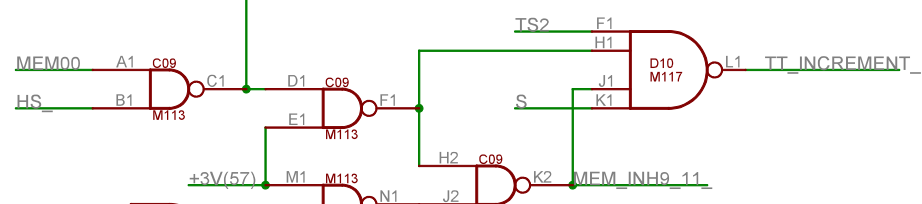
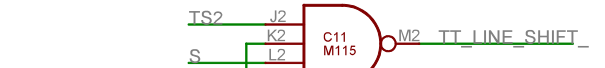
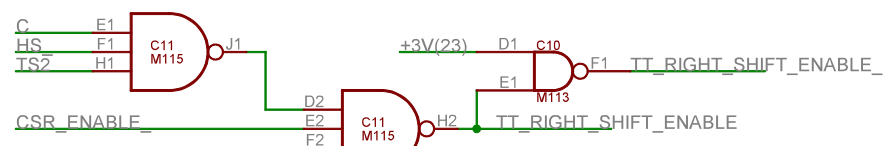
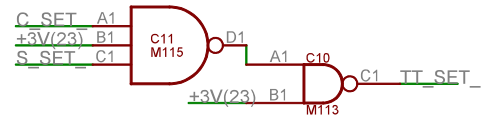
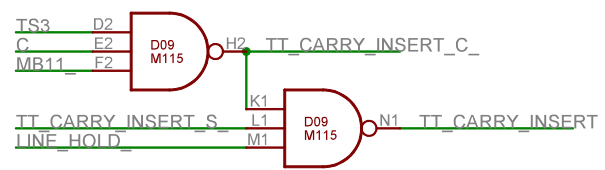
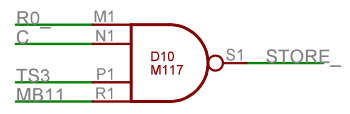
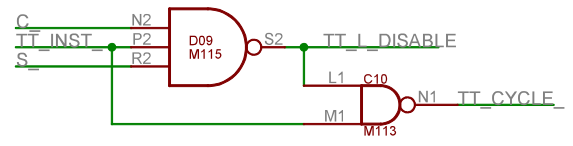
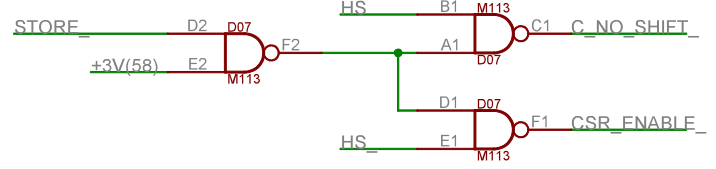
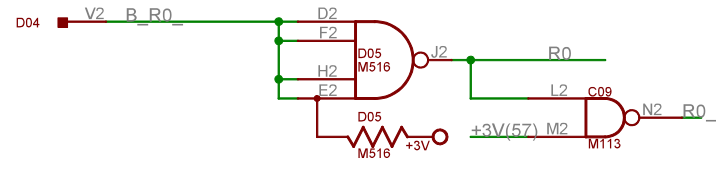
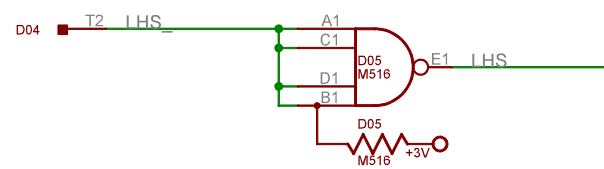
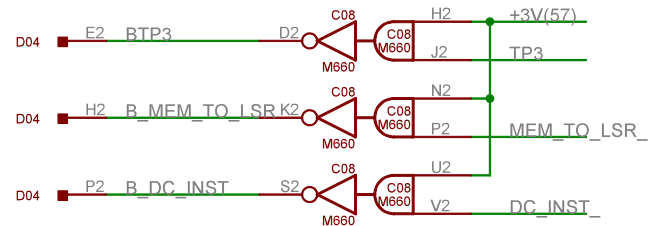
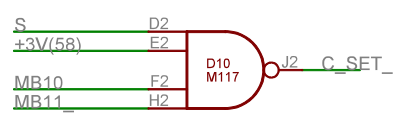
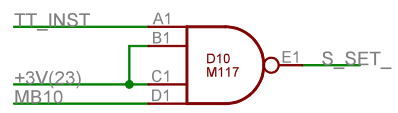
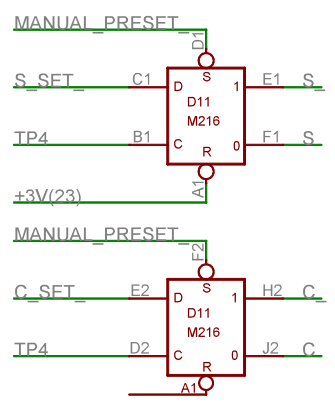
<b>D-BS-ke8i-0-2 EAE Control</b>	
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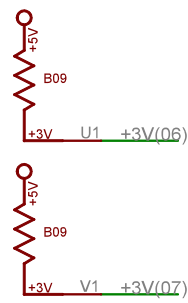
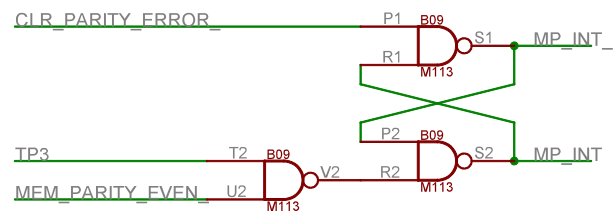
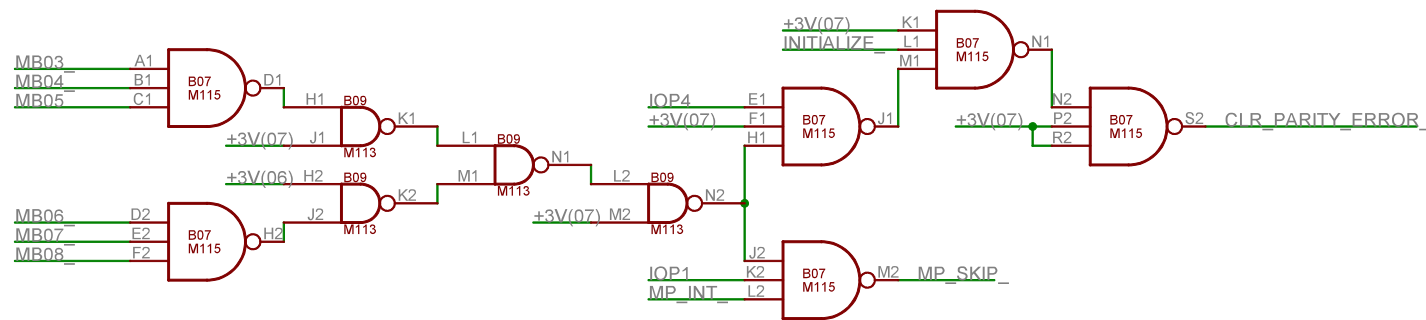
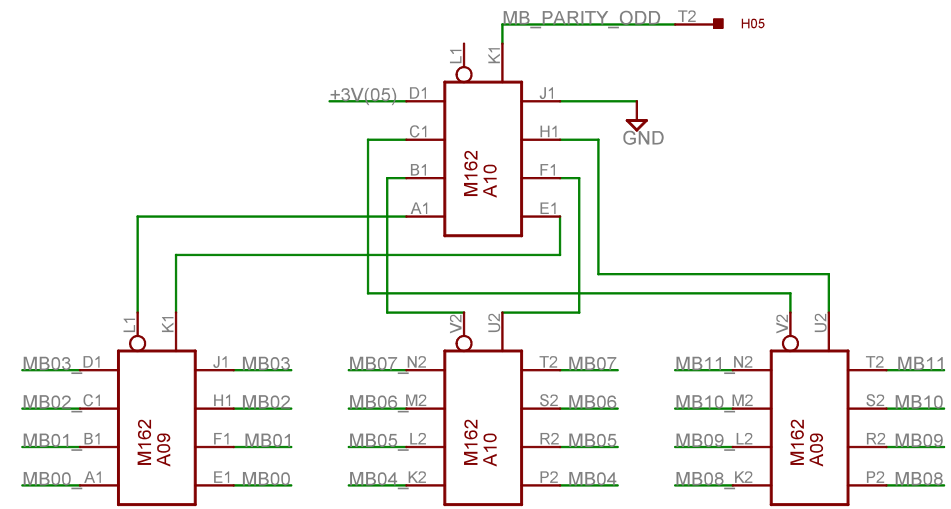
D-BS-ke8i-0-3 Multiplier Quot. and Step Counter

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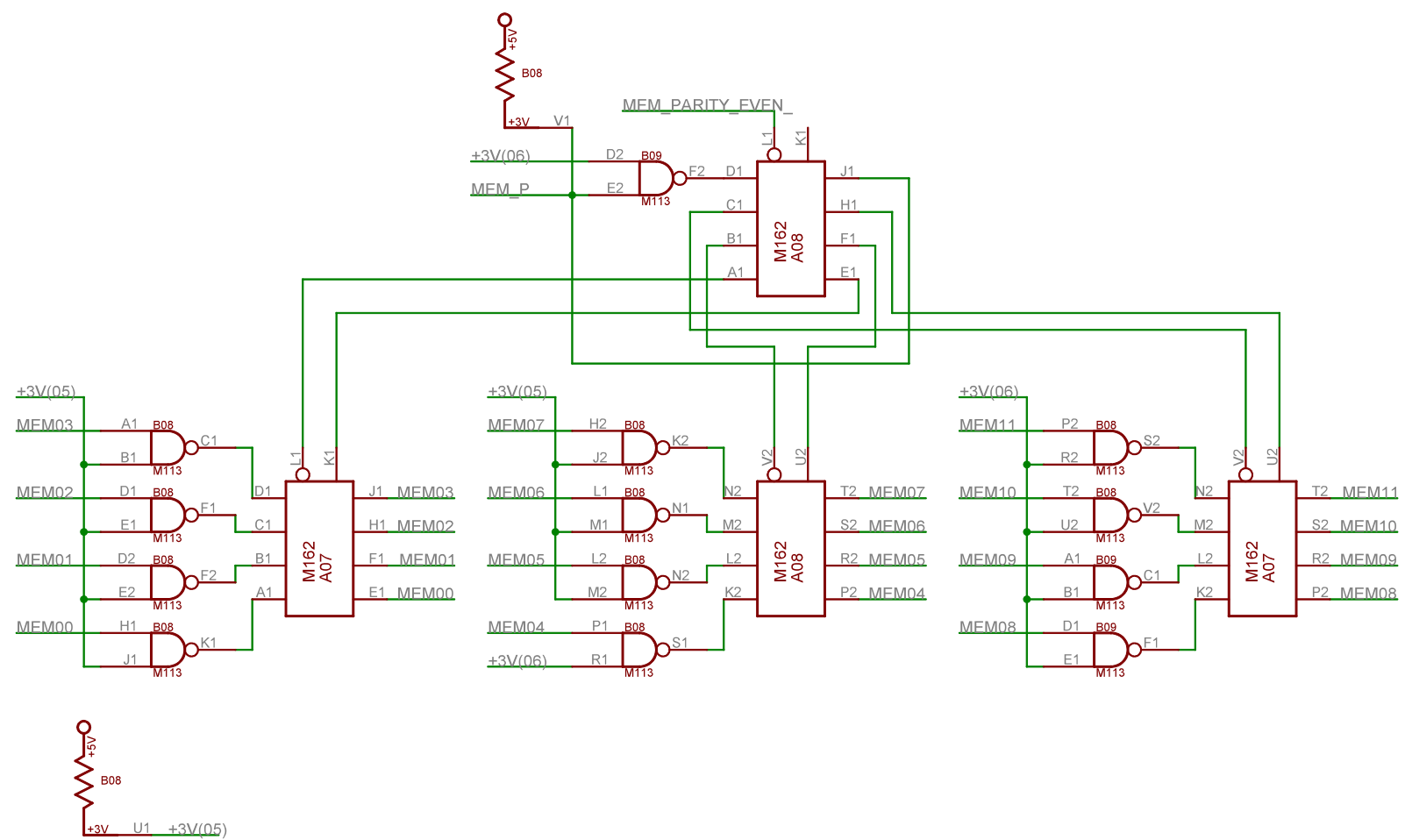


<b>D-BS-dl8i-0-2 Data Line Interface</b>	
TITLE: pdp8i-dec	
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GND

D-BS-mp8i-0-1 Memory Parity Option (1/2)	
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D-B5-mp8i-0-1 Memory Parity Option (2/2)

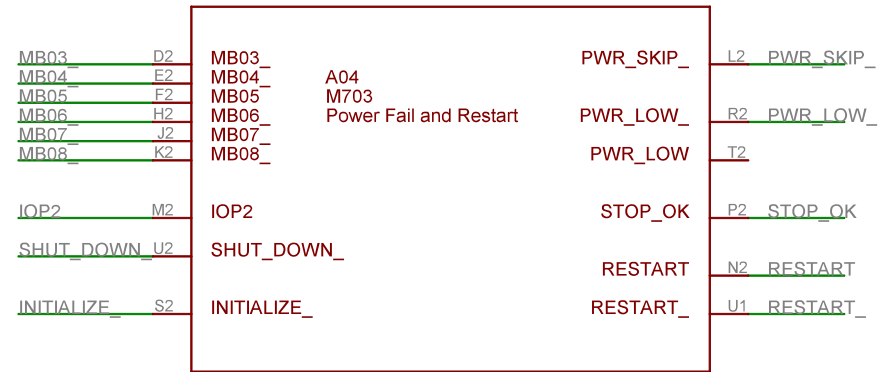
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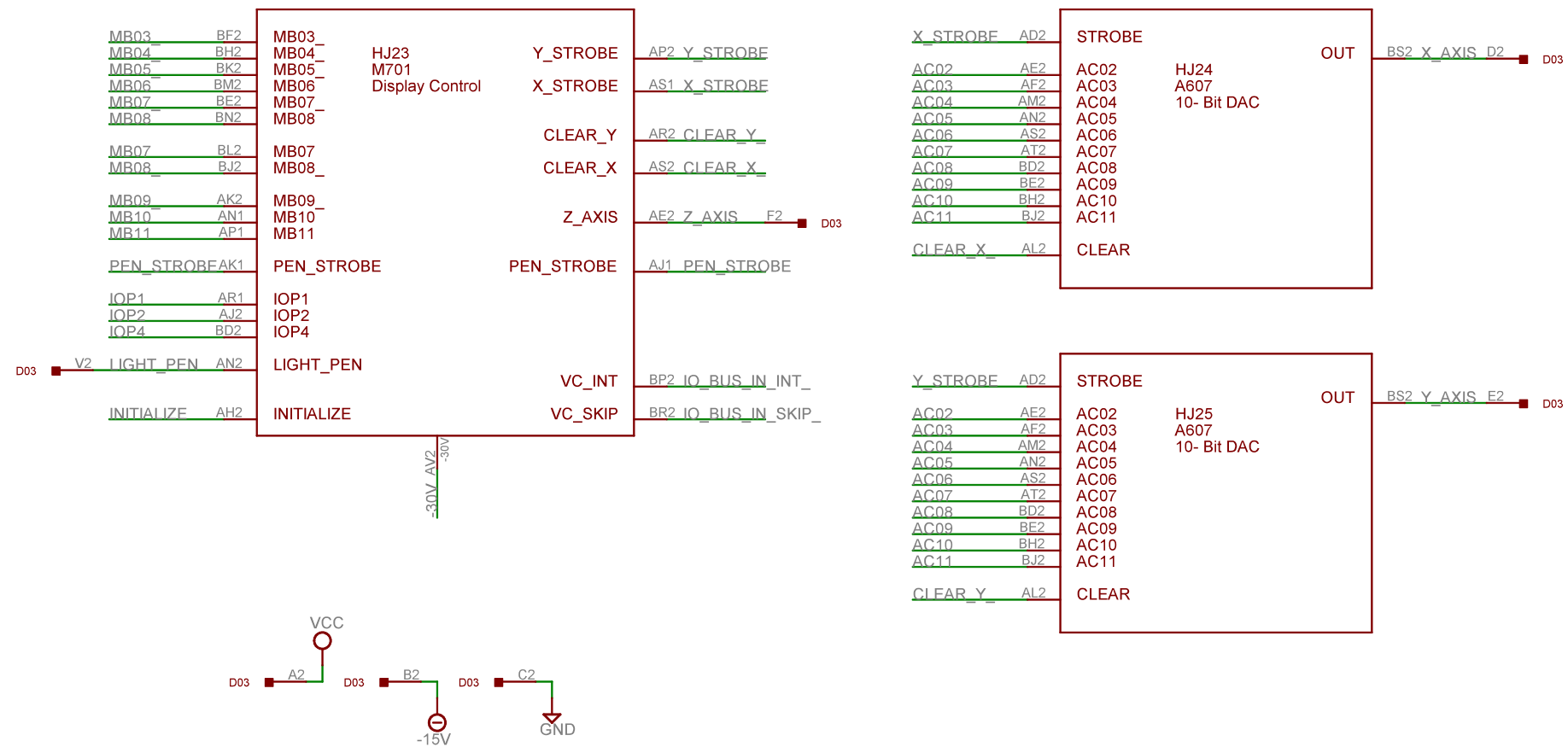
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D-BS-vc8i-0-1 Display Control

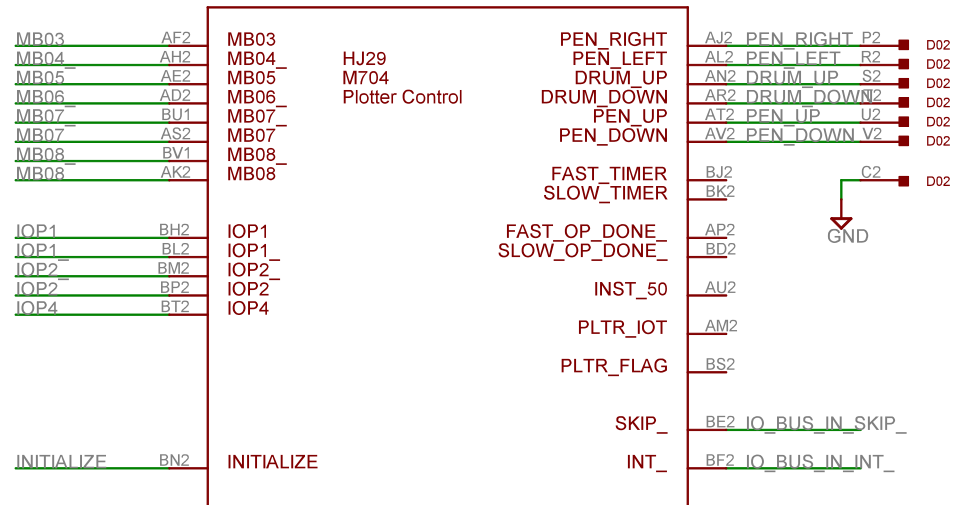
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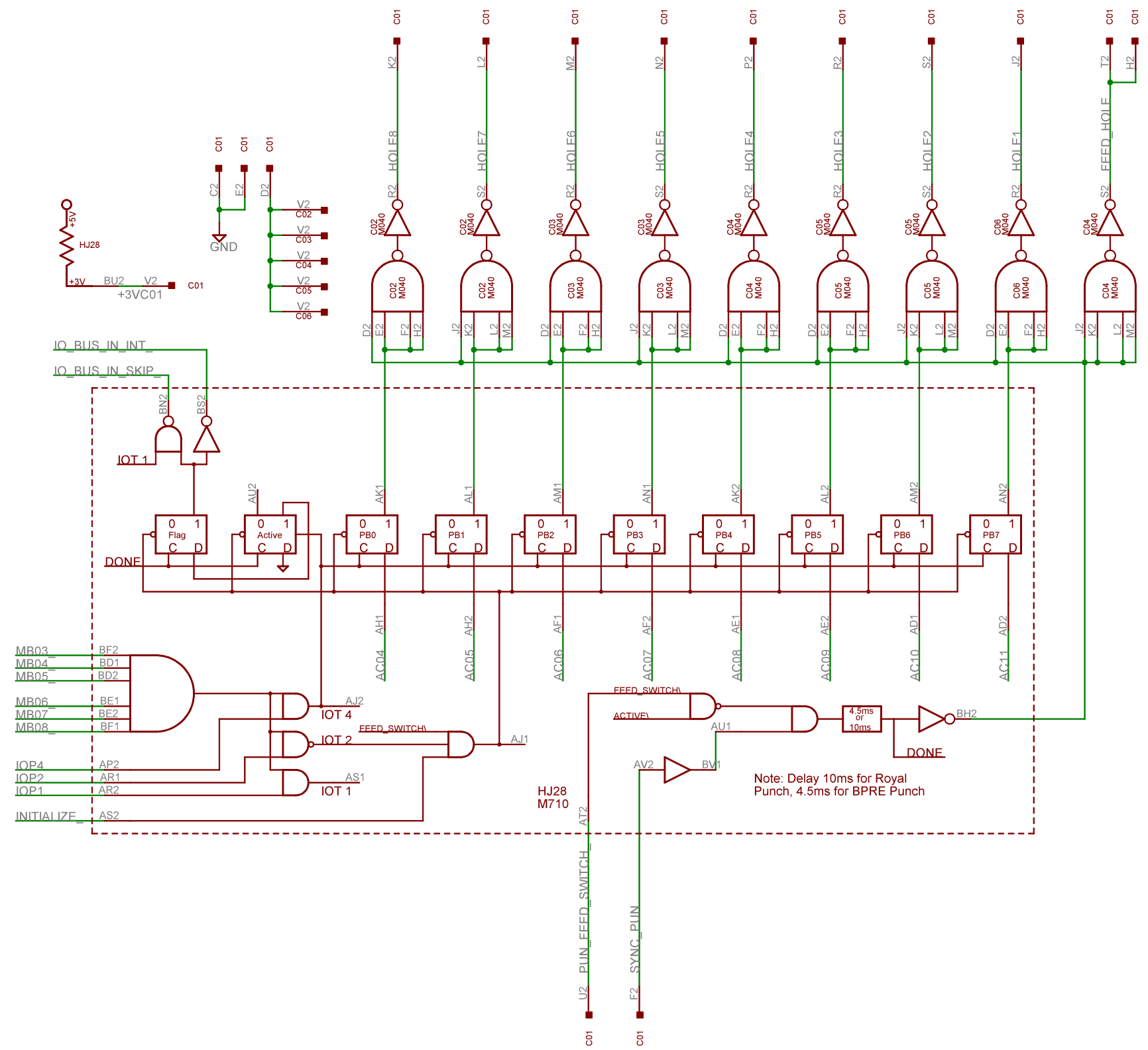
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D-BS-pp8i-0-1 High Speed Punch

TITLE: pdp8i-dec

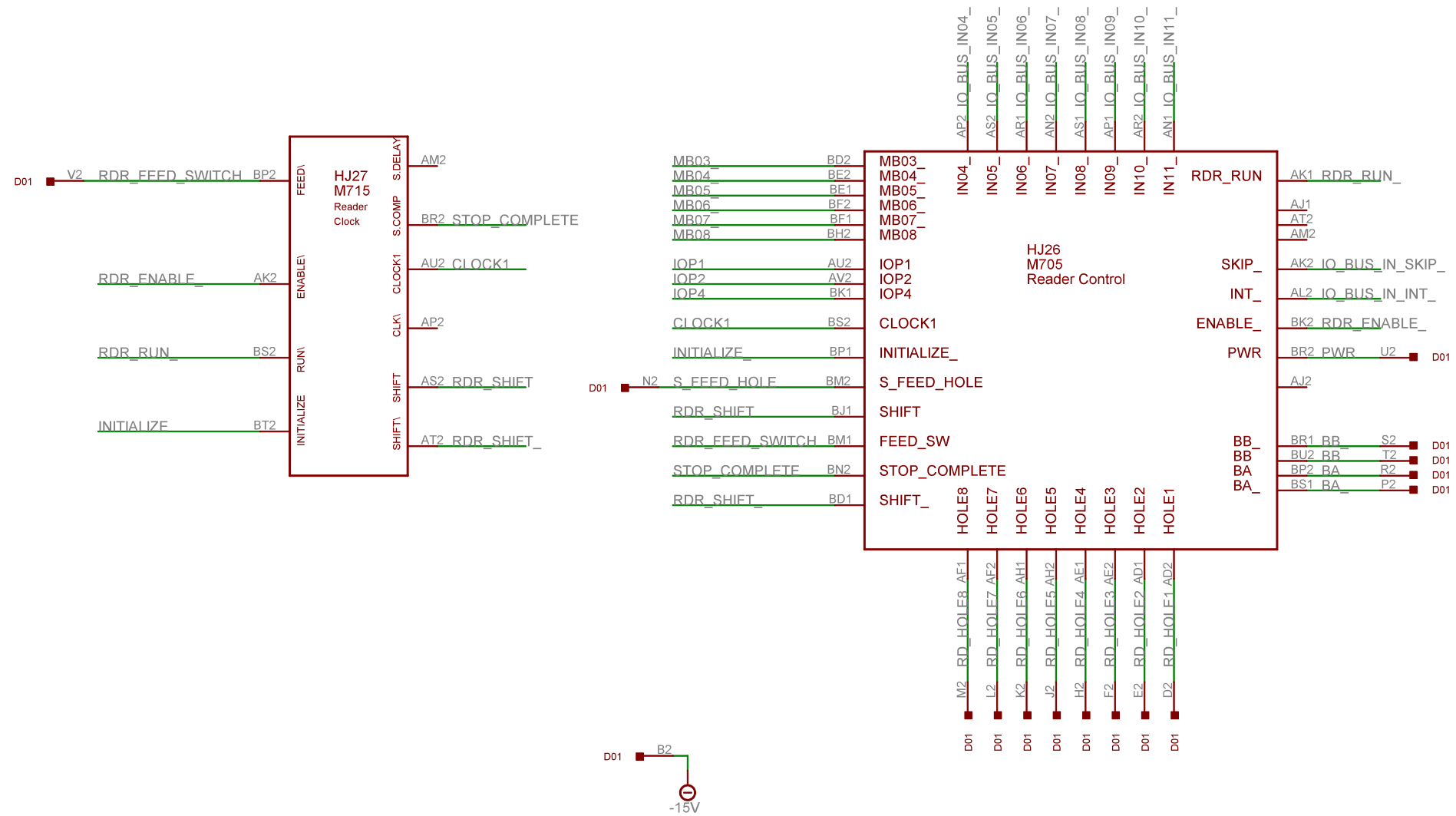
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D-BS-pr8i-0-1 High Speed Reader

TITLE: pdp8i-dec

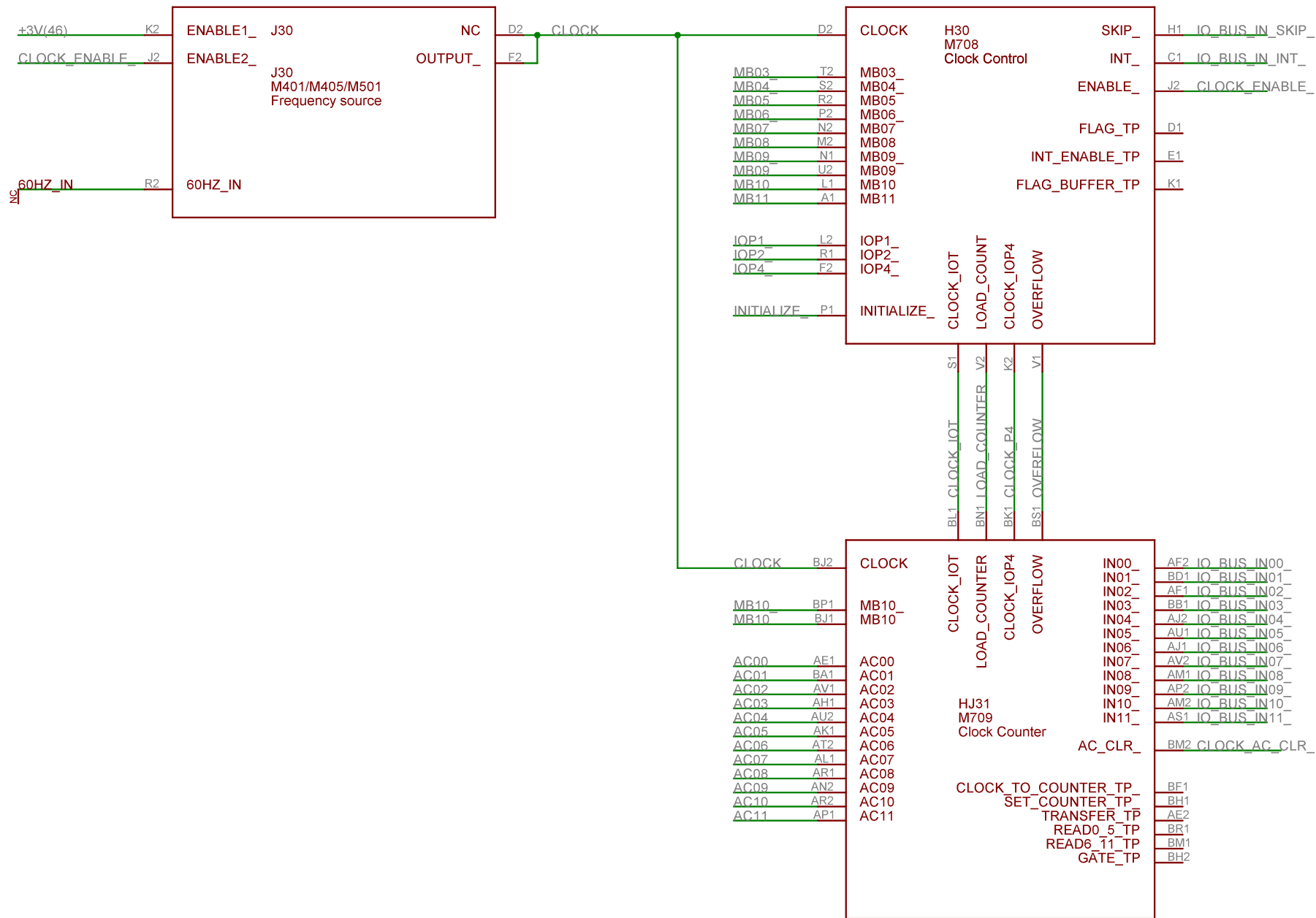
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D-BS-kw8i-0-1 Real Time Clock Option

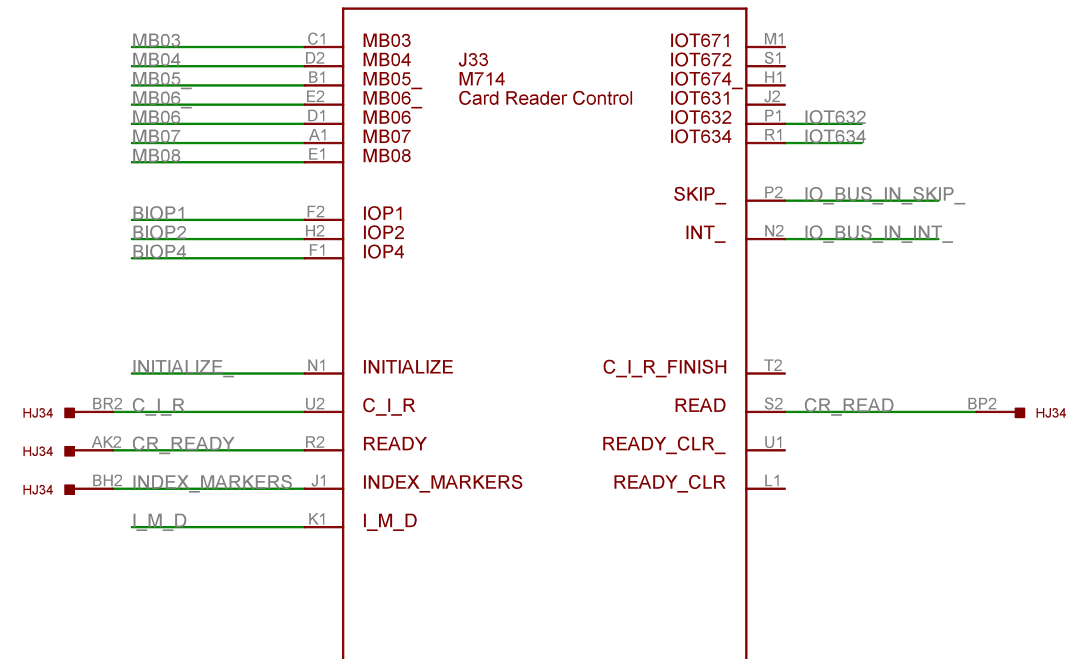
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D-BS-cr8i-0-2 Card Reader Control #1

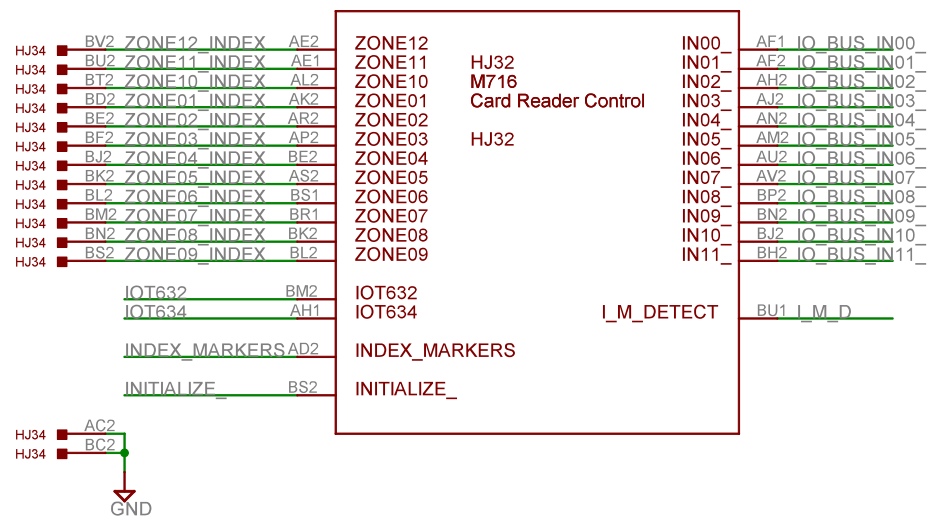
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