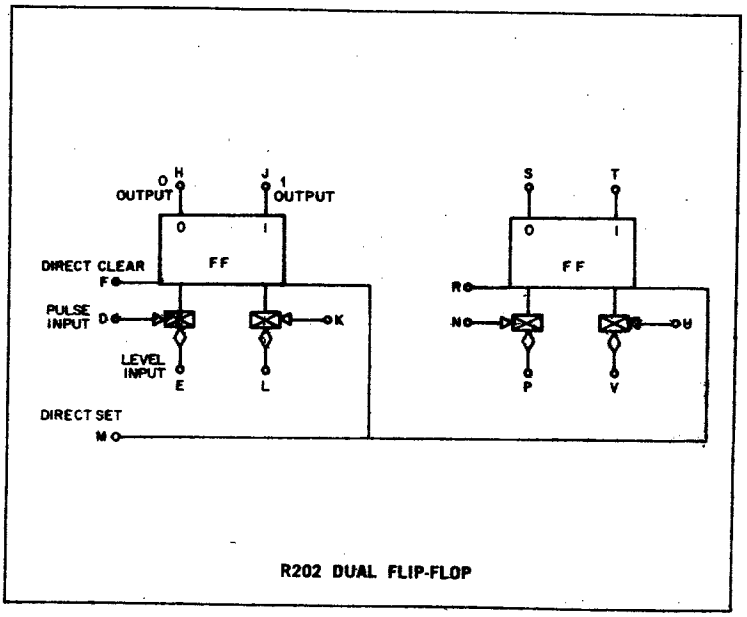
DUAL FLIP-FLOP
TYPE R202

R SERIES



R202 DUAL FLIP-FLOP

The R202 Dual Flip-Flop contains two identical flip-flops. Each has a direct clear input, a common set input, and two DCD gates. The R202 can perform in any one of the following applications without additional gating: up counter, down counter, shift register, ring counter, jam transfer buffer, and switch tail ring counter.

INPUT: Direct Set and Clear — A standard 100 nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma for each clear input, and 2 ma for the set input. When not in use, the direct terminals must be at —3v. If the flip-flop is in an up counter with carry gates enabled, direct clear pulses must be at least 400 nsec long to suppress carry propagation. In like manner, a 400 ns set pulse must be used when the flip-flops are arranged as a down counter. If both inputs are held at ground, both outputs are at —3v. **DCD Gates, Level** — Standard levels of —3v and ground. Because DCD gates are internally conditioned by the state of the flip-flop, a complement input may be formed by tying the 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. When 1 and 0 DCD gates are connected in parallel to form a complement input, the total level load is 3 ma at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground) at any frequency up to 2 mc. It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input, as in complementing or shifting, the total pulse load is 4 ma at ground. **Collector Triggering** — The flip-flop can also be set or cleared through its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal (6 ma each).

OUTPUT: Standard levels. The carry propagate time is 70 nsec. Each terminal can drive 15 ma of external load at ground and has an internal load of 6 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1 v within 80 nsec after the flip-flop is pulsed.

Note: Additional driving capability at —3v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10 v(A)/0.5 ma, —15 v(B)/34 ma.

R202 — $25.00