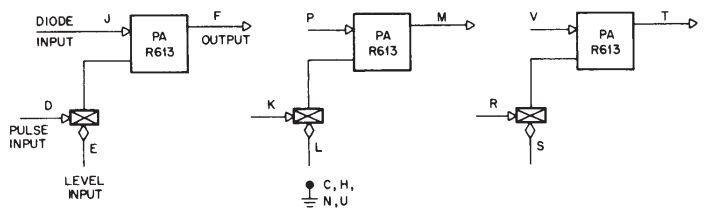
R613 PULSE AMPLIFIER

Standard Size FLIP CHIP Module, 18 Pins



The R613 is pin compatible with and functionally similar to the R603.

Each pulse amplifier produces a 200 ns R-series (positive) pulse. A DCD gate and a diode input permit considerable flexibility. Input pulses can occur at any rate up to 2 MHz. Delay through the pulse amplifier is typically 50 ns.

INPUTS: DCD Gate Level - DEC standard levels of -3 V and ground. The DCD gate is enabled by a ground level and disabled by a -3 V level. The conditioning level must be present for at least 200 ns before the gate is pulsed. The level input represents 2.5 mA of load at ground and 0 mA at -3 V. The level input is prevented from going above ground by a diode clamp.

DCD Gate Pulse - 40 ns or longer pulses going from -3 V to ground at any repetition rate up to 2 MHz. It can also be driven by positive going level changes (-3 V to ground) with rise times of 60 ns maximum and durations of 40 ns minimum. The input must have been at -3 V for at least 200 ns prior to operation of any input. The pulse input represents 5 mA of load at ground, 0 mA at -3 V. The pulse input is prevented from going above ground by a diode clamp.

Diode - DEC standard levels of -3 V and ground. 40 ns or longer pulses or positive going level changes (-3 V to ground) with a rise time of 60 ns maximum will trigger the PA. The input must be returned to -3 V for at least 400 ns before another input is allowed to trigger the PA from either the DCD gate or diode input. The output produced by a ground level at the diode input will be at ground for 200 ns or as long as the input is at ground, whichever is longer. This feature can be used to apply a dc clear to flip-flops during an initial power-up period and also to apply clear pulses during normal operation. The diode input represents a 1 mA load at ground.

OUTPUTS: Outputs are positive pulses (-3 V to ground) of from 190 ns to 350 ns duration or levels (see diode input above). Each output can supply 65 mA at ground. The internal clamped load supplies -3.5 mA at -3 V. Output pulses may be ORed by paralleling PA outputs. The outputs are buffered so that the PA cannot be triggered by noise on the output line (or by another gate or PA). Pulse lines and grounds should be kept as short as possible.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+8 V to +12 V	3.3 mA
B	-15 V	-12 V to -18 V	77 mA
C,H,N,U	ground		

Pins C,H,N, and U must all be grounded.