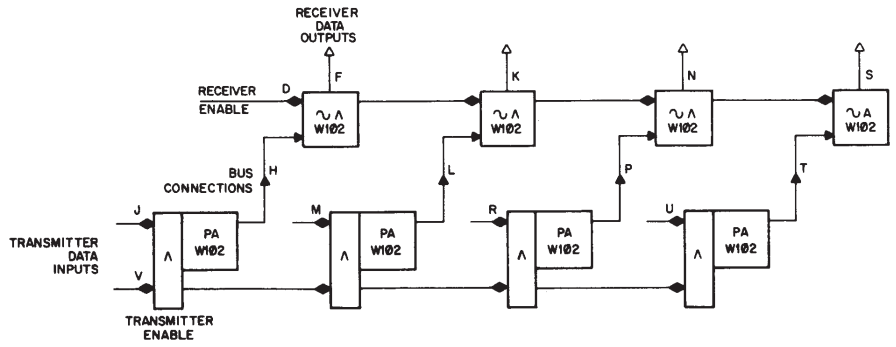
W102 PULSED BUS TRANSCEIVER

Standard Size FLIP CHIP Module, 18 Pins



The W102 module is a pulsed bus transceiver capable of communicating with the PDP-1-D, PDP-6 and the PDP-10 memory bus system.

INPUTS: Transmitter Inputs - 2 mA per circuit shared between the grounded inputs; 2 mA maximum for data inputs; 8 mA maximum for the enable input. No load at these inputs at -3 V.

Receiver Inputs - 2 mA per circuit shared between the grounded input. No load at -3 V. The receiver pulse input is tied to the transmitter output, hence internally the pulsed bus. The bus is loaded by 2 mA at ground when the enable input is negative. The enable input draws 8 mA maximum at ground. The receiver gate is a modified diode gate with additional noise rejection at ground.

OUTPUTS: Transmitter Outputs - This module is designed to drive a single 50 Ω cable or two 100 Ω cables. Cables must be terminated in their characteristic impedance so that the load at the transmitter output is 50 Ω. The output pulse is 100 ns nominal width (100 to 125 ns at nominal supply voltage) and -3 V in amplitude, with no positive overshoot. A pulse is produced whenever both inputs to a transmitter circuit are negative. Either the transmitter inputs or the enable input may be pulsed. The input pulse must be at least 30 ns wide and should not occur more often than 400 ns (2.5 MHz maximum repetition rate). Input pulses or levels that are longer than 100 ns make the output pulse up to 15% longer than for a minimum width input pulse.

Receiver Outputs - The receiver outputs are pulled to ground whenever the receiver enable is at -3 V and the bus is pulsed (whether by the same module or by some other source). The outputs should be used with a clamped load to drive additional diode logic or to set unbuffered flip-flops via their collectors. The receiver outputs should not be used to gate emitters as the upper level is too negative to insure adequate noise rejection. ORing of the receiver with other collectors at ground is allowable. The receiver output will suppy 29 mA at ground.

TECHNICAL NOTES: The W102 does not adversely affect the pulsed bus operation even though its power supplies are turned off.

When connecting a large number of transceivers (10 or more) to a bus, the upper (ground) level of the bus is pulled down by the receiver idle current (approximately 2 mA per enabled receiver). To compensate for this effect, the 100 Ω (or 50 Ω) terminating resistors can be returned to a slightly positive voltage (not more than +1.5 V) to make the bus rest at ground. A diode should be connected so that the bus itself will not go above +0.7 V. The bias supply should be thoroughly bypassed to ground. When only one or two receivers are enabled at a time, this scheme is not necessary.

The wires connecting the W102 to the transmission line should be as short as possible; these lines carry large signals at high impedances and are subject to cross-talk. The transmission line is defined as the path of wire from the "left end" terminator (through many cabinets and much cable) to the "right end" terminator.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to +20 V	0.6 mA
B	-15 V	-8.5 V to -23 V	85 mA (26 mA at low duty factor)
C	ground		

NOTE

This description applies to modules revision F or later.
For information on earlier modules contact DEC.

APPLICATION: Typical connections of the W012 are shown in the Figure 4-8.

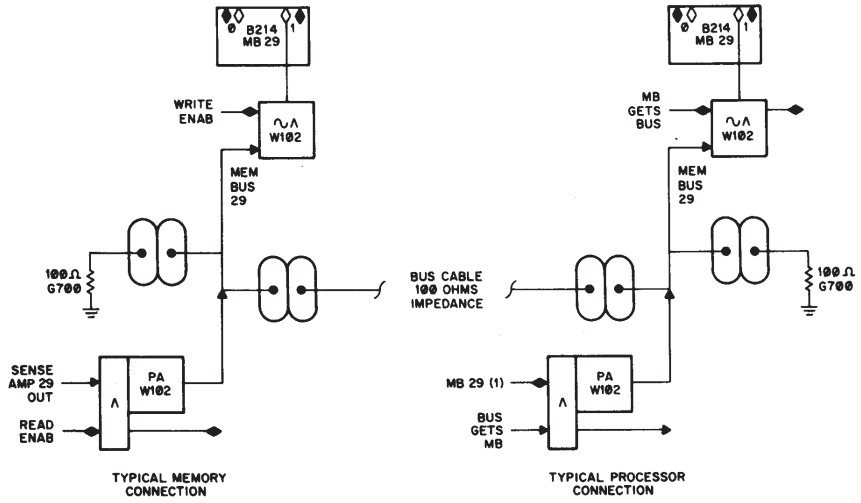


Figure 4-8 Typical Connections, W102