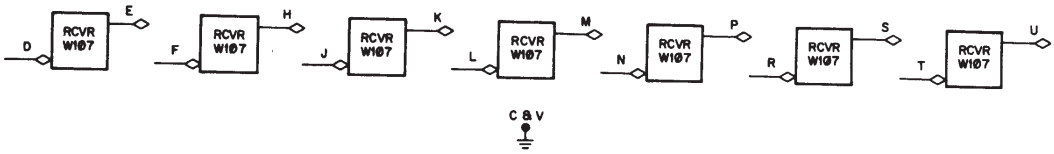
W107 I/O BUS RECEIVER

Standard Size FLIP CHIP Module, 18 Pins



The W107 contains seven identical non-inverting receiver circuits with high-impedance input for buffering signals from the PDP-10 I/O Bus. The W107 is pin compatible with the W500 emitter follower.

INPUTS: Standard DEC levels of -3 V and ground. Each input draws 0.22 mA at ground and less than 1 μA at -3 V.

OUTPUTS: Standard DEC levels of -3 V and ground. Each output can supply -7 mA at -3 V and 36 mA at ground, in addition to the internal clamp load. The TTT is less than 150 ns for both rise and fall.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	2.5 V to 17.5 V	.14 ma
B	-15 V	-10 V to -20 V	100 mA
C,V	ground		

Both pins C and V must be grounded.