Atmel PLD Design Guidelines

Introduction

This application note provides guidelines for designing with Atmel PLDs and answers many frequently asked questions. Many of the issues described are fundamental design practices common to all digital logic, and are included here in reference to programmable logic devices. Except where a specific device is mentioned, the guidelines apply to all Atmel PLDs. Following these guidelines will help to ensure that the device will function as designed in an application. Worst-case timing analysis should be performed for all designs. This will guarantee that the device will function correctly under the complete temperature and voltage ranges.

Clocks

Clocking is one of the most important aspects of any digital design. Care should be taken to make sure that input clock signals have fast, clean edges and are glitch-free. All registers in Atmel simple PLDs (16V8, 20V8 and 22V10) have the same clock. Atmel CPLDs (such as the ATV750B, ATV2500B and ATF1500 family) have many different clock options, which provide design flexibility, but could add potential timing problems.

Global Pin (Synchronous) Clocks

Global (or synchronous) clocks are the simplest and most predictable. A single master clock, driven by an input pin, is used to clock every flip-flop. This provides the fastest clock-to-output delay and minimum skew between registered outputs.

Product Term (Asynchronous) Clocks

In all Atmel CPLDs, each register clock may use a product term. This option allows the designer to generate individual clocks for each register. It also means that the clock to the register can be a function of more than one signal. This adds a great deal of flexibility in the design, but it also adds potential timing problems.

Gated Clocks

Some of Atmel's CPLDs also offer a gated synchronous clock option. This means that the global clock signal can be gated with a product term function. This provides the best of both clock options: the timing advantages of the global clock and the flexibility of a product term clock. The gating function is implemented differently in different devices. For example, in the ATV2500B, the global clock and the product term are simply ANDed, as shown in Figure 2. This means that the product term input is not a true clock enable. In the timing diagram shown in Figure 1, the input CKEN changes from low to high while the global clock signal CLK is high, generating a clock edge at the register (CK). This may cause the register to clock unexpectedly.

In the ATF1500 family of devices, a product term is used to generate a clock enable signal. Anytime the clock enable is low the global clock input is ignored. When the clock enable goes high, the next global clock rising edge will clock the register. The ATF1500 clock enable schematic and timing waveforms are shown in Figures 3 and 4.

Atmel PLD Design Guidelines

Application Note

Rev. 0790C–09/00

Figure 1. ATV2500B Gated Synchronous Clock Timing Waveforms

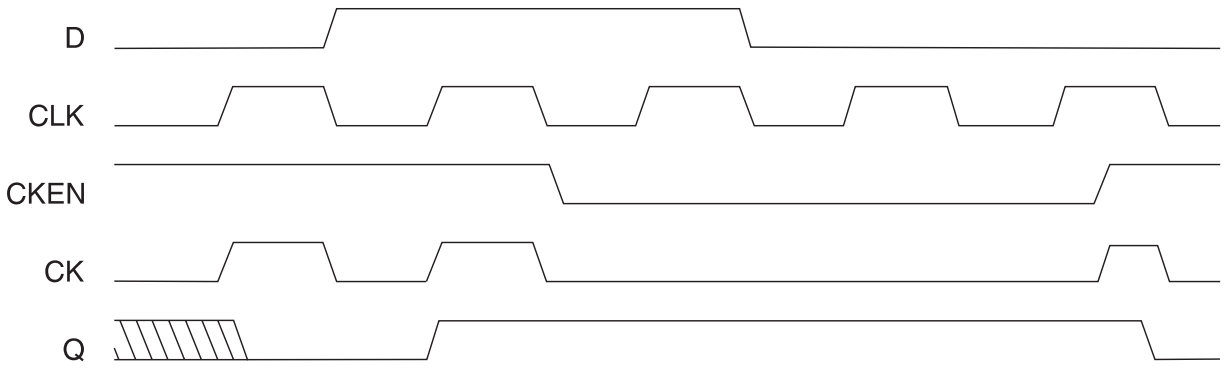


Figure 2. ATV2500B Gated Synchronous Clock Schematic

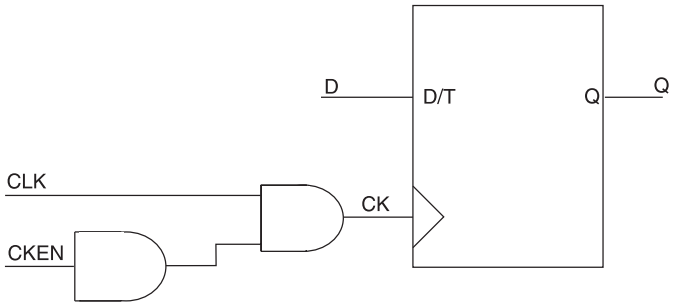


Figure 3. ATF1500 Register with Clock Enable Schematic

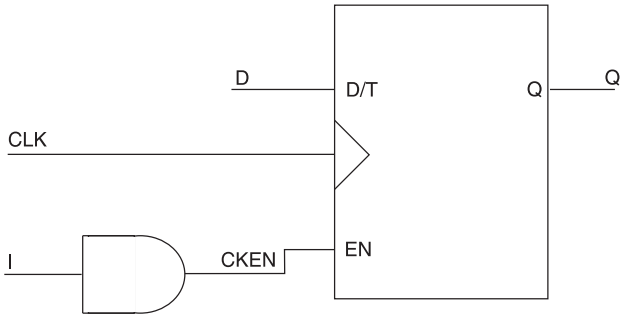
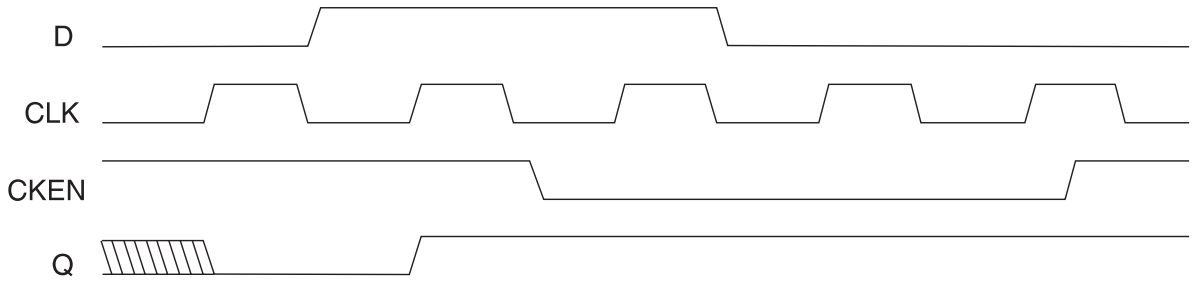


Figure 4. ATF 1500 Register with Clock Enable Timing Waveforms



Clock Timing

The timing for each register will depend how it is clocked. Separate timing parameters are provided for pin (synchronous) and product term (asynchronous) clocks. In general, pin clocked registers will require longer setup time, no hold time and have a faster clock-to-output delay. Product term clocked registers will require a shorter setup time, require a positive hold time and have a slightly longer clock-to-output delay. The skew between registered outputs is also affected by the choice of pin or product term clocks. An example which demonstrates the difference in timing between pin and product term clocks is shown in Figure 5.

Multi-Level Clocks

It is generally not recommended that clock signals be generated using more than one level of logic gates. This can introduce potential race conditions and timing problems, which may not be apparent without extensive timing analysis. The delays between gates in the device may be slightly different while still meeting the minimum and maximum timing parameters. Signals generated in different parts of the device may have different delays due to the difference in the lengths of the internal paths, creating potential race conditions. If many signals must be used to generate a clock signal, it is preferable to used a gated synchronous clock or a clock enable.

Minimum Clock Slew Rate

It is critical that incoming clock signals have a minimum slew rate of 0.1 V/ns (0V to 5V in 50 ns). Slow rising clock edges may cause registers to clock incorrectly or "double clock" (particularly troublesome in counters or state machines). A signal with slow rising edges can be buffered externally with a schmitt trigger buffer.

Note: Atmel "L" (low-power) and "Z" (zero-power) devices depend on input signal transitions to "wake" the devices. The devices may not respond to extremely slow edges (more than 7200 ns/volt) at the appropriate time. Refer to the application note "Saving Power with Atmel PLDs" for more information on Atmel "L" and "Z" devices. Contact Atmel PLD technical support if an application requires signal edges with slew rates less that 0.1 V/ns.

Reset and Preset

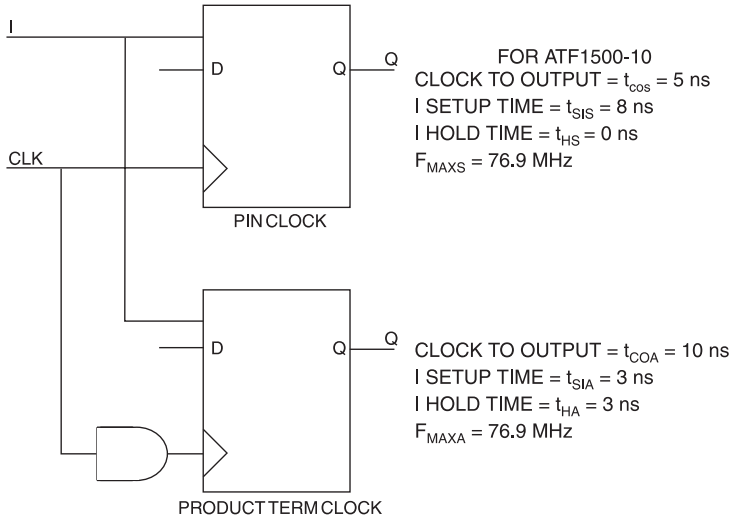
Global vs. Product Term

As with the clocks, many Atmel CPLDs offer the option of using either a global input pin or a product term to generate register resets or presets. The global pin reset provides fast synchronous register resets and in some devices can save product term resources, but limits the design flexibility. Product term resets and presets provide ultimate flexibility, but may have slower timing characteristics. The polarity of the reset or preset signals depends on the device (refer to the databook for specifics). The state of a registered output following a reset or preset will depend on whether the programmable polarity control is used. Refer to the application note "Using Programmable Polarity Control" for more details.

Asynchronous vs. Synchronous

If a register has an asynchronous reset or preset, no clock is required to toggle the register when the reset/preset is asserted. A synchronous reset or preset requires a rising clock edge after the reset/preset line is asserted in order to reset/preset the register. As with any synchronous operation, minimum set up and hold times are required.

Figure 5. Pin vs. Product Term Clock Timing



Minimum Pulse Width

Each product's datasheet specifies minimum reset and preset pulse widths for asynchronous control signals. This is the minimum length of time the reset/preset signal must be asserted in order to guarantee that the register resets/presets correctly. However, smaller pulse width on the reset/preset line may cause the register to change state, even if it is less than the specified minimum pulse width.

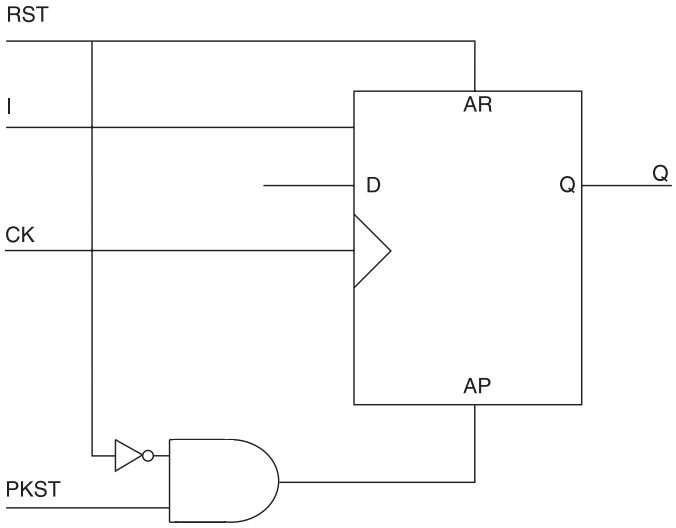
Recovery Time

For devices which have asynchronous resets or presets, each datasheet also specifies a reset/preset recovery time. This is the time during and after the reset/preset signal is asserted that the register should not be clocked. If the recovery time is violated, the register may not reset/preset correctly.

Asserting Both Reset and Preset

Asserting both the reset and preset signals simultaneously can cause unpredictable results in a register. In some devices it may even cause a metastable condition, with the output of the register eventually settling to either high or low. For the Atmel V-series PLDs, the reset is asynchronous and the preset is synchronous. In this case, the reset will override the preset (the device will immediately reset whenever the reset is asserted). For the F1500 family of PLDs, both the reset and preset are asynchronous, so the state of the register is undetermined. It is a good design practice to write the logic equations so that both reset and preset cannot be asserted simultaneously. Additional logic can be implemented to prioritize the reset and preset signals, as in the example shown in Figure 4. In this example, anytime the reset is asserted, the preset will be disabled.

Figure 6. Logic to Eliminate Reset/Preset Conflicts



Output Enable

Global vs. Product Term

All Atmel CPLDs provide individual product terms for the output enables. This provides maximum design flexibility. Some devices also offer a global output enable which is driven by an input pin. This may be desirable if large buses are enabled/disabled with the same signal, because it will minimize the skew between the outputs, and in some devices save logic resources.

Timing

Careful timing analysis should always be performed on tri-state buses to ensure that there is no bus contention. Bus contention can cause a device to temporarily draw excessive current, which in extreme cases may result in damage to the device. Timing parameters are provided for both enabling and disabling the output buffers. For devices which have both pin and product term output enable options, the output enable timing is specified for each option.

Refer to the application note "Tips on Using Test Vectors for Atmel PLDs" for information on creating test vectors to test bi-directional I/O pins.

Other Timing Issues

Hazards

A hazard is a condition where a circuit may generate a glitch, causing erroneous circuit operation.

The glitch may occur when an input changes, but the output is not expected to change state, or while the output is changing state. Hazards may be caused by a race condition, when multiple inputs to a logic function are changing simultaneously. Differences between the input propagation delays may cause the output to temporarily change state. A race condition can occur any time the stability of a circuit output depends on the change of more than one input.

One example where a race condition can cause a glitch is the transparent latch circuit shown in Figure 7. Figure 8 is a schematic of the latch. As shown in Figure 9, when both the data input (D) and the latch enable (LEN) are high, the latch is transparent and the output (Q) will be high. When LEN goes low, product term B will go high, and Q will stay high. However, if the delay from the product term A going low is shorter than the delay from product term B going high, Q will glitch low.

Another example of a design with a potential hazard condition is a state machine where multiple state bits change during a state transition. Since in an actual design the bits do not change at exactly the same time, an output which is decoded from the current state could glitch as the state machine briefly appears to be in another state. Figure 8 shows an example of a Moore state machine with a potential hazard. In the transition from state B to state C, the state machine may briefly appear to be in state A or D, depending on which state bit changes more quickly. This would cause a glitch on the output signal (OUT).

It is important to identify and eliminate hazard conditions which may affect circuit operation. This is especially crucial if the output of the circuit will be used as a clock. Potential hazards can be identified with careful timing analysis. A minimum propagation delay of zero should be used if no minimum is specified, and a skew between all signals should always be assumed.

Figure 7. Race Condition in a Latch-Schematic

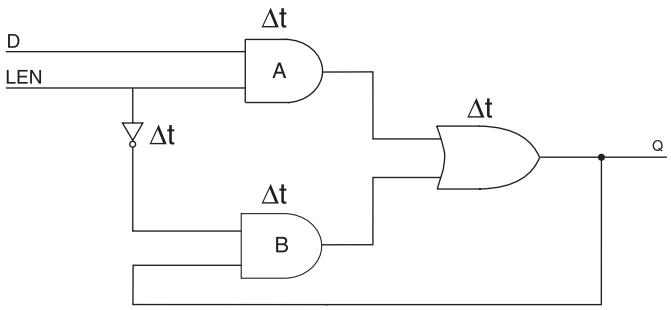
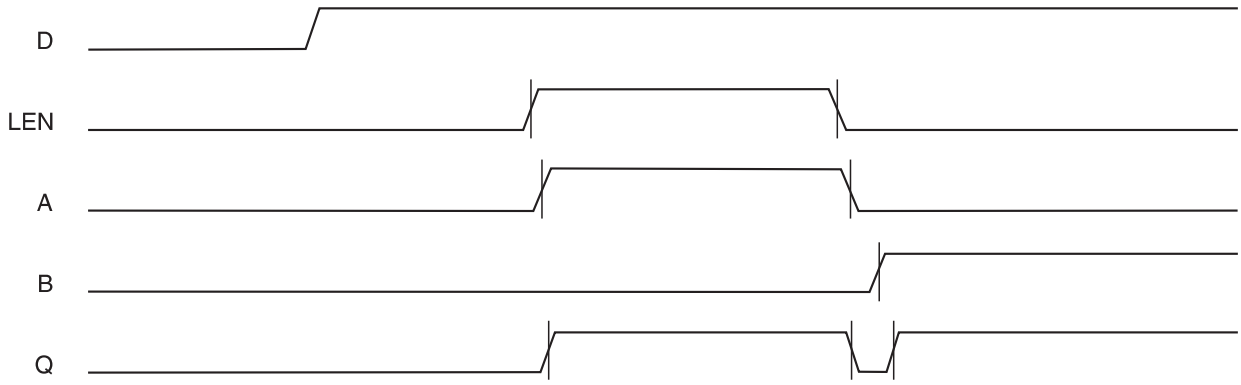


Figure 8. Race Condition in a Latch-Timing Waveform

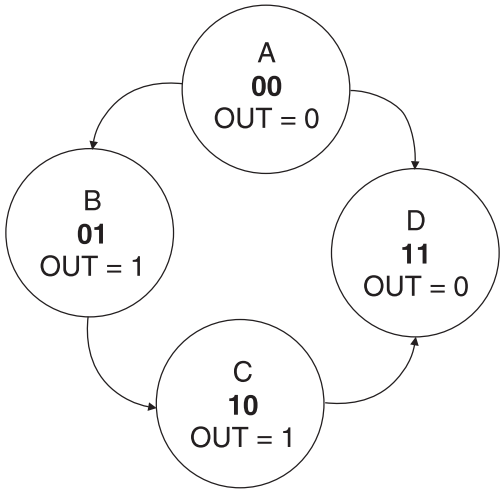


Most hazards can be eliminated with changes in the logic. One way is to buffer the glitchy output through a register or latch. Transparent latches are available in the ATF1500 CPLD family. This gives the signal time to settle before it is captured. If the hazard is caused by multiple inputs changing at the same time, it may be possible to change either the timing or sequence of the inputs.

In the case of the state machine from Figure 8, the state bit assignments could be assigned so that only one state bit changes with each state transition. Figure 9 shows the state machine with the modified state bit assignments. With only one state bit switching on any transition, there is no possibility of an output glitch.

Another way to eliminate potential hazards is to provide redundant logic. In PLDs this is usually implemented as an additional product term which ensures that the output is not dependent on particular input(s) when they are transitioning. Figure 10 shows the latch example from Figure 7 with

Figure 9. Hazard in a State Machine Output



redundant logic added to eliminate the hazard. The extra product term (C) assures that Q will stay high when the latch enable signal transitions low. Since most logic compilers by default try to eliminate redundant logic in order to reduce the number of product terms, such equations need to be identified with compiler directives. Refer to your compiler software manual for details on retaining redundant product terms.

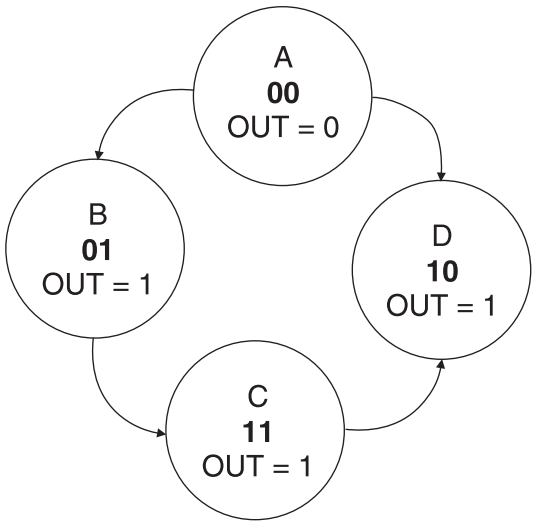
Minimum Delays

As with any timing parameter, a minimum delay should never be assumed in timing calculations, unless they are specified in the datasheet. If not specified, the minimum should be assumed to be zero. In the ATF1500 family, foldback logic should not be used to create a minimum delay. Delays can vary significantly with temperature, voltage and device processing. Maximum delays occur under worst-case conditions and are tested. Minimum delays occur under the best-case conditions, and may be significantly less than the maximum value.

Skew

Signals generated on different I/O pins invariably have some skew. This skew is caused by a difference in the physical path which different signals take within the device. There is no way to calculate the skew between two signals, since it will be greatly dependent on temperature, voltage, output loading, etc. Signals from adjacent pins with similar output loads will usually have the smallest skew, typically less than 500ps for output loads equivalent to those used for AC testing.

Figure 10. Modified State Machine



High-to-Low vs. Low-to-High Transitions

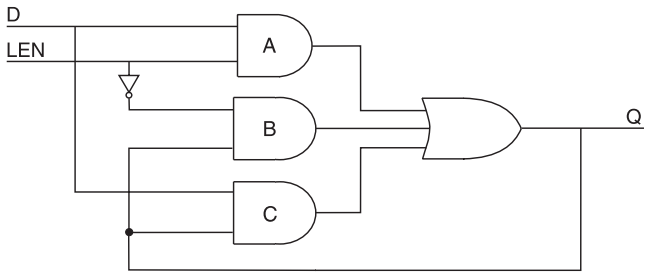
In some device data sheets, timing parameters are specified for both high-to-low and low-to-high transitions. This is due to the differences in the device switching. In any critical timing analysis, especially with potential race conditions, both the high-to-low and low-to-high should be considered. For timing parameters which do not specify a high-to-low or low-to-high transition, the maximum is for the worst case transition. For example, if the t_{PD} is specified to be 10 ns (max), it may be 10 ns for a high-to-low transition, but only 8 ns for a low-to-high transition.

Using Latches

The registers in the ATF1500 family can be configured as D- or T-type flip-flops or as transparent latches. These latches can be very useful for buffering asynchronous inputs or for buffering outputs which may otherwise be subject to logic glitches, as described earlier. If a latch function is desired, it is preferable to use the register latch configuration. Foldback logic should not be used to create a cross-coupled NAND type of latch. Differences between the low-to-high and high-to-low transitions create a race condition which may cause the latch to function incorrectly.

In other PLD devices which do not have register latch configurations, two combinatorial outputs may be used to create a cross-coupled NAND latch. If the device has programmable slew rate control, make sure that the output slew rates are consistent, minimizing the skew between the outputs.

Figure 11. Glitchless Latch Using Redundant Logic



Power-up Considerations

V_{CC} During Power-up

In order to assure that the devices power-up correctly, it is important to follow the power-up sequence and timing described in the datasheets. It is important that V_{CC} start below 0.5V and rise monotonically. If V_{CC} starts above 0.5V or does not rise monotonically problems may occur during the device power-up configuration or in the power-up reset.

The ATF150XASV Series has two options for the hysteresis about the reset level, V_{RST}, Small and Large. To ensure a robust operating environment in applications where the device is operated near 3.0V, Atmel recommends that during the fitting process users configure the device with the Power-up Reset Hysteresis set to Large. Atmel POF2JED users should include the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, an additional condition is added: If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

I/O Voltage Levels Relative to V_{CC}

The maximum V_{IH} levels are specified in each device data sheet. For most 5-volt devices, the V_{IH} maximum is V_{CC} + 0.75V. For 3-volt or wide voltage devices, the V_{IH} maximum is around V_{CC} + 0.5V. For any device, V_{IH} should not be applied to an I/O pin when the device is not powered-up (V_{CC} is removed). This may cause the device to try to power-up through that pin and may cause damage or improper power-up sequence. V_{IH} applied to an input-only pin while the device is not powered-up may or may not have the same effect, but is generally not recommended. For power-sensitive applications, an alternative to removing V_{CC} to save power, use devices with the power-down pin mode (devices power down to the µA range).

Power-on Voltage Level

Each device will power-up once V_{CC} has crossed a certain voltage level, specified as V_{PRST}. For 5-volt devices, the power-on voltage is typically around 3.8V. For 3-volt and wide-voltage devices, it is around 2.7V. These are typical levels, which may change with temperature and device processing variations.

I/Os During and After Power-up

During power-up, all I/O pins on Atmel SPLDs and CPLDs will be tri-stated until V_{CC} reaches the power-on voltage level. This is to prevent bus contention during power-up. Once the device is powered-up, the state of the I/O pins will depend on how the device is programmed and the state of the inputs. For registered I/Os, the register will be reset internally. For devices with pin-keeper circuits, all pins will be in an undetermined state (low or high) until V_{CC} reaches the power-on voltage level.

Power-up Reset

In all Atmel PLDs, the registers reset on power-up (assuming the correct power-up sequence and timing are followed). For SPLDs (16V8, 20V8), there is a fixed inverter between the register and I/O pin, so the I/O pins will be high following power-up. For the F1500 family, the I/O pins will be low following power-up. For the 22V10 and V-series devices, the polarity of the I/O pin is programmable, so the state of the I/O pin depends on whether the I/O is programmed as a buffer or inverter. For devices with a pin-keeper circuit, if the I/O pin is disabled, the pin-keeper will cause the signal to be held either high or low (will not float).

Problems Associated with Incorrect Power-up and Power-down

Some Atmel PLDs load configuration data from the configuration bits into internal latches (to save power) when the device powers up. **In order to assure that the correct configuration is loaded, V_{CC} must start below 0.5V and rise monotonically**. I/O signals should not rise faster or before the V_{CC}, as this may cause the device to power-up through that pin and may cause a configuration failure.

Since the power-up sequence may take microseconds on some devices (but never longer than the specified t_{PRST}), it may take a device that long to respond to external signals. If the device is clocked during power-up, the registers may not reset correctly. It is generally not a good design practice to rely on the power-up reset circuit to get registers to a known state, since it is often difficult to guarantee that clock signals will not toggle during system power-up. It is preferable to create a system reset signal which can be asserted following power-up.

During power-up, many of Atmel's L devices require the same Icc as standard power devices. Once V_{CC} has crossed the power-on voltage level (see the individual device data sheets), the L mode will become active, and the I_{CC} will drop to the specified standby current. During normal operation, decoupling capacitors can provide the necessary transient current when the devices switch from the standby to active mode. But since the capacitors aren't charged until after power-up, the power supply must be able to supply enough current to power-up the device.

When powering down Atmel PLD devices such as the ATF1500 family, ATF16V8C and ATF22V10C, the V_{CC} and I/O pin voltages must go below 0.5V before powering the devices back up. Otherwise, incorrect configuration data may be loaded.

Pin-keeper Circuits

Some Atmel PLDs have active pin-keeper circuits on the I/O and input pins. Diagrams of the pin-keeper circuits are shown in Figure 9. These circuits help assure that a pin stays in the last logic state when the pin is no longer being driven. The pin-keeper circuit typically requires approximately 40-50 µA to be overdriven. Therefore, the circuit can be easily overdriven with a 50k pull-up resistor to the 5V supply. The pin-keeper circuit by itself should not be relied on for a bus pull-up. If external bias resistors must be used on pins with pin-keeper circuits, **Atmel recommends a 50k (or less) pull-up to V_{CC}, or a 20k (or less) pull-down to ground.**

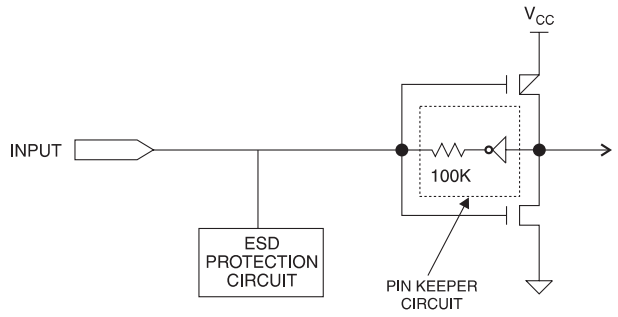
On power-up, if the I/O pin is disabled, the pin-keeper will cause the signal to be held either high or low (will not float), but the state is not guaranteed. In some devices (e.g. ATF1500A) the pin-keeper circuit is programmable and can be disabled.

Using Low-power ("L") Devices

Atmel's low-power ("L") PLD devices can provide significant power savings by automatically switching the device to a standby mode when the inputs are not changing. However, the devices require the same current as standard-power devices when in the active mode. This current can typically be supplied by the charge stored on decoupling capacitors. Atmel recommends a 0.2 µF capacitor connected across each V_{CC} and ground pin set (some CPLDs have multiple V_{CC} and GND pins). Refer to the application note "Saving Power with Atmel PLDs" for more information on power calculations and designing with "L" devices.

The timing parameters for the "L" devices include the wake-up delays. This means that the worst case timing analysis does not need to include additional delays for the wake-up. The device will meet the maximum delays whether it is in an active or standby mode. It should be noted that the propagation delays when the device is already awake will be less than the propagation delay when the device is in a standby power mode. For synchronous designs, this should not be a problem, but may cause a potential problem in asynchronous designs. The timing of a circuit may change depending on whether the device is in an active or standby mode when one of the inputs changes. The only way to guarantee consistent propagation delays is to assure that the device is always in an active mode (although it defeats the purpose of using a low-power device).

Figure 12. Pin Keeper Circuit Diagrams



Using Zero Power ("Z") and Pin-controlled Power Down Devices

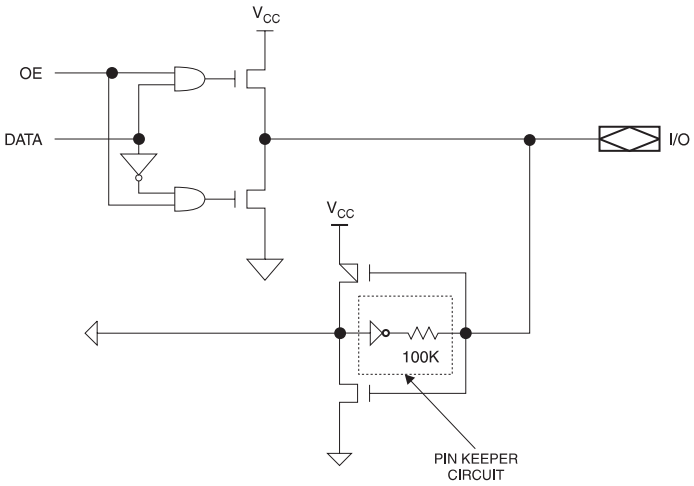
Atmel also offers zero power ("Z") devices. These devices switch to an edge-controlled microamp-range power standby mode. The device automatically detects when the inputs are not changing and switches to the standby mode. For edge-controlled zero power devices the "wake-up" delays are included in the regular timing parameters. As with the "L" devices, the propagation delay for the "Z" devices when the device is already awake will be less than the delay when the device is coming out of the standby mode.

For pin-controlled power down devices, one of the input pins is configured as a power-down pin. Anytime the pin is asserted, the device will switch into a zero power standby mode, and ignore all inputs. For the pin-controlled power down mode the delays for the device to switch into and out of the standby mode are specified as separate parameters in the data sheet.

Like the "L" devices, the "Z" devices require standard power device current levels when in the active mode. This current can be supplied by the decoupling capacitors. Refer to the application note "Saving Power with Atmel PLDs" for more information on power calculations and designing with "Z" devices.

Reducing Internal Noise

In order to ensure that a PLD will operate as designed, it is important to try to minimize both internal and system noise. Both the board layout and the logic design can affect the internal noise.



Unused Pins

Atmel's Flash devices (ATF16V8, ATF20V8, ATF22V10, F1500 series) devices have either pull-up resistors or pin-keeper circuits on all input and I/O pins, so unused pins do not require external resistors. Atmel's EPROM devices (AT22V10, V-series CPLDs) do not have input or I/O pull-up resistors. Any device pins which are left floating can cause internal noise and increase power consumption. Unused input pins should be pulled-up, using a 50k (or less) resistor. Unused I/O pins should be pulled-up or programmed to output a logic high. If left unprogrammed, they will default to tri-state.

Ground Bounce

Ground bounce is a result of multiple outputs switching simultaneously, causing a large current to flow to the device ground. Due to the inherent inductance on an IC's ground pin(s), the device ground current cannot change without inducing a voltage. The result is a shift in the device's internal ground level, causing voltage spikes on other quiescent low-state outputs. In the worst case, the spikes can exceed the 0.8V V_{IL} level and cause other circuits to detect a transition. This effect is aggravated by any external inductance, such as wires or socket leads, between the device's ground pin(s) and the board ground plane.

Ground bounce can be minimized by reducing the number of outputs or registers which switch simultaneously, and by reducing the inductance between the ground pin(s) and the system ground. For the ATF1500 family devices, the outputs can be set to a slower slew rate, reducing the peak switching current and the resultant ground bounce.

Decoupling Capacitors

It is very critical that decoupling capacitors be placed very close to each supply pin on the device. Decoupling capacitors supply transient currents during switching. In the case of the "L" and "Z" devices, standard power device current levels are required when the device is in the active mode. Without the capacitors, the V_{CC} may droop, causing erratic behavior. Please refer to the application note "Selecting Decoupling Capacitors for Atmel's PLDs" for more information on specific types and values of capacitors.

Power and Ground Connections

Most PLD devices which are larger than 24 pins have multiple power and ground pins. It is critical that all power and ground pins are connected directly to power or ground planes on the board. Any unconnected power or ground pins may cause the part to function incorrectly. Wires or traces used to connect the supply pins to the system ground or sockets will increase the inductance along the supply path, and increase the supply noise and ground bounce.

Reducing System Noise

Transmission Line Effects

Transmission line effects can cause many problems in high speed logic circuits. The most common transmission line problem with CMOS devices is ringing due to a voltage reflection. This is due to the fast output slew rates, large voltage swing and high input impedances. The ringing appears as voltage undershoot and overshoot when an output transitions. In some cases, the undershoot or overshoot may be large enough to cause an input to detect another transition, for example causing a register to double clock.

Another common problem is the transmission line's voltage divider effect, due to the finite impedance of the driving source output impedance and the characteristic impedance of the transmission line. When the device switches, the voltage at the source end of the transmission line may remain at an indeterminate logic level until the reflected wave returns from the other end of the transmission line. This at best creates timing ambiguity, and at worst may cause improper operation of any load device(s) located near the source end of the transmission line.

Another transmission line problem is timing skew due to the propagation delay along the transmission line. This can create a significant reduction in system performance, as it will require longer data setup and hold times for sequential logic. It can also create race conditions which may result in logic glitches.

There are several ways to reduce the problems associated with transmission lines. First, the length of the traces or wires should be kept as short as possible. This will reduce the time it takes for the wave to be reflected. It will also minimize the voltage divider effect and wire propagation delays. For long lines, some form of termination may be required. The type of termination (series, parallel or pullup/pulldown) will depend on the system requirements. If there is more than one load on the line, the distribution of the loads (either lumped at the end of the line or distributed along the line) will determine the type of termination that can be used. Some transmission line effects can also be reduced by slowing the output slew rate using the programmable slew rate control available on some devices.

Metastability

One of the problems associated with asynchronous designs is metastability. This is a condition caused by indeterminate logic levels within a latch circuit. It is manifested by an indeterminate level or oscillations on the output signal. This can be caused by an input changing during the setup and hold period around a clock transition or by a clock pulse shorter than the minimum required duration. The output will eventually settle to a stable state, but not until after the normal delay time.

In order to avoid outputs which go into a metastable state, asynchronous inputs should be synchronized using additional registers. An example showing how to synchronize inputs is shown in Figure 12. If an input violates the setup or hold time, it will cause a metastable event on the output of the first register, but settle before the next clock. The inputs to the final register will then be synchronous to the clock and the output will be stable.

State Machines

PLDs are ideal for implementing state machines, since they provide wide fan-in and an abundance of product terms. In order to make sure that the state machine is robust, it is important to consider the state on power-up and what would happen if the state machine should inadvertently enter an unused state. All of the registers in Atmel PLDs will reset on power-up, as long as the correct power-up sequence and timing are followed. The state of the outputs or feedbacks may depend on the polarity of the macrocell. It is generally preferable to provide a master reset to the state machine following power-up, which will force it to a reset or idle state. Any unused states should cause the state machine to branch to a reset or idle state.

Figure 13 shows a state machine with a master reset and an unused state which is defined to branch to the reset state on any clock cycle.

Conclusion

Following the guidelines presented in this application note will help to create PLD designs which are reliable and which function as designed in the application. The designer should also perform functional simulation, worst-case timing analysis and vector testing to pinpoint any potential problems before the PLD is integrated into the system.

Figure 13. Synchronizing Asynchronous Inputs A and B

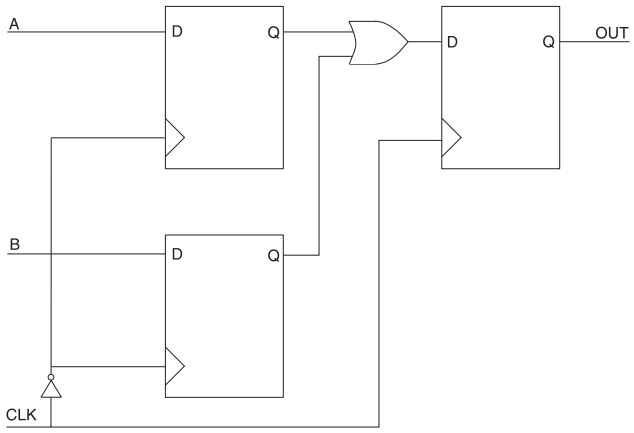
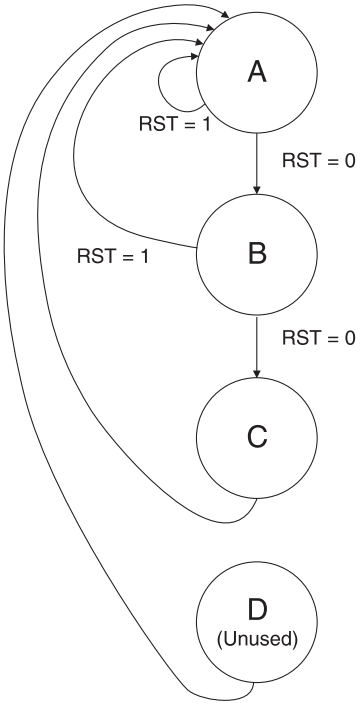


Figure 14. Robust State Machine



Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-803-000
FAX (44) 1355-242-743

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex
France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

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