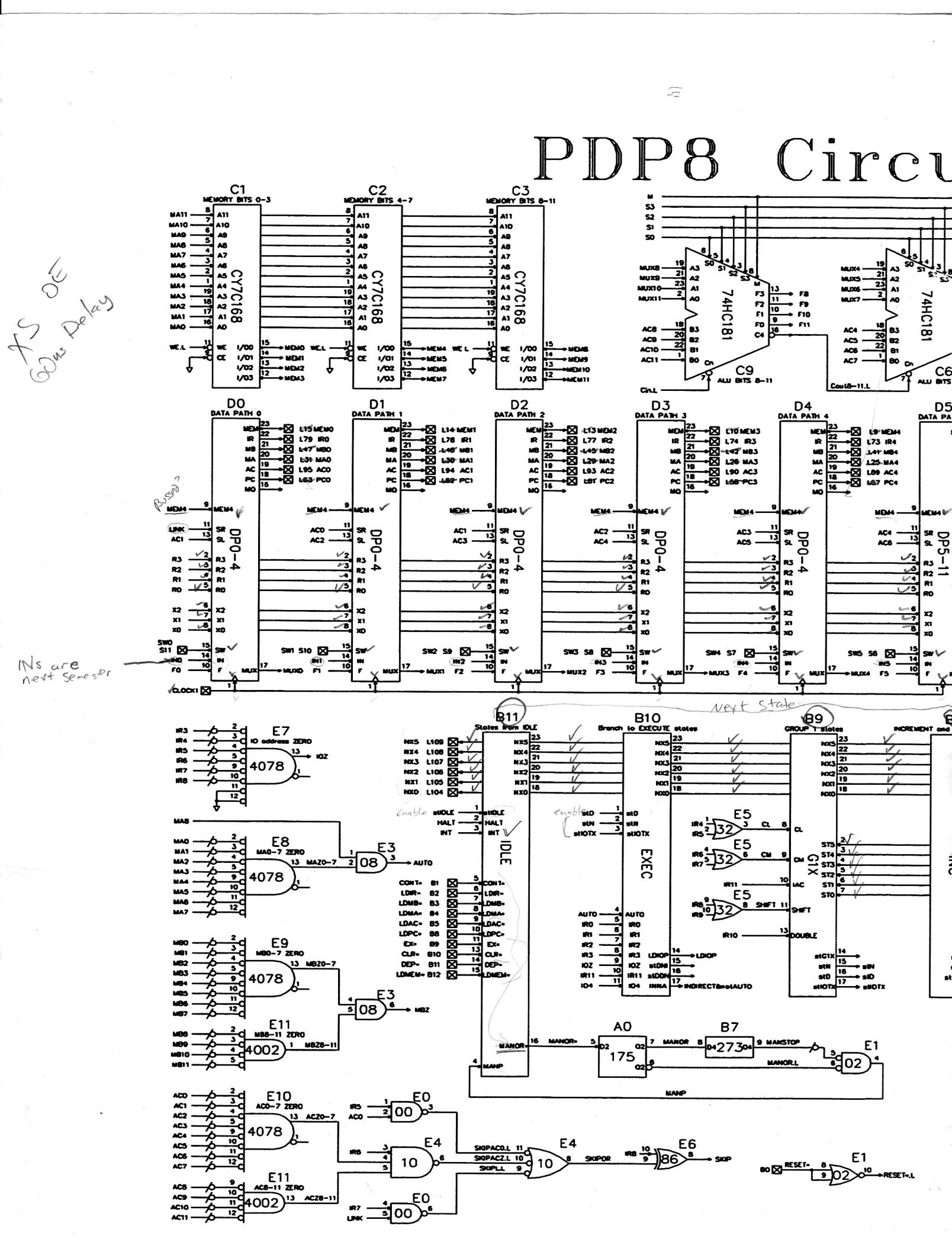
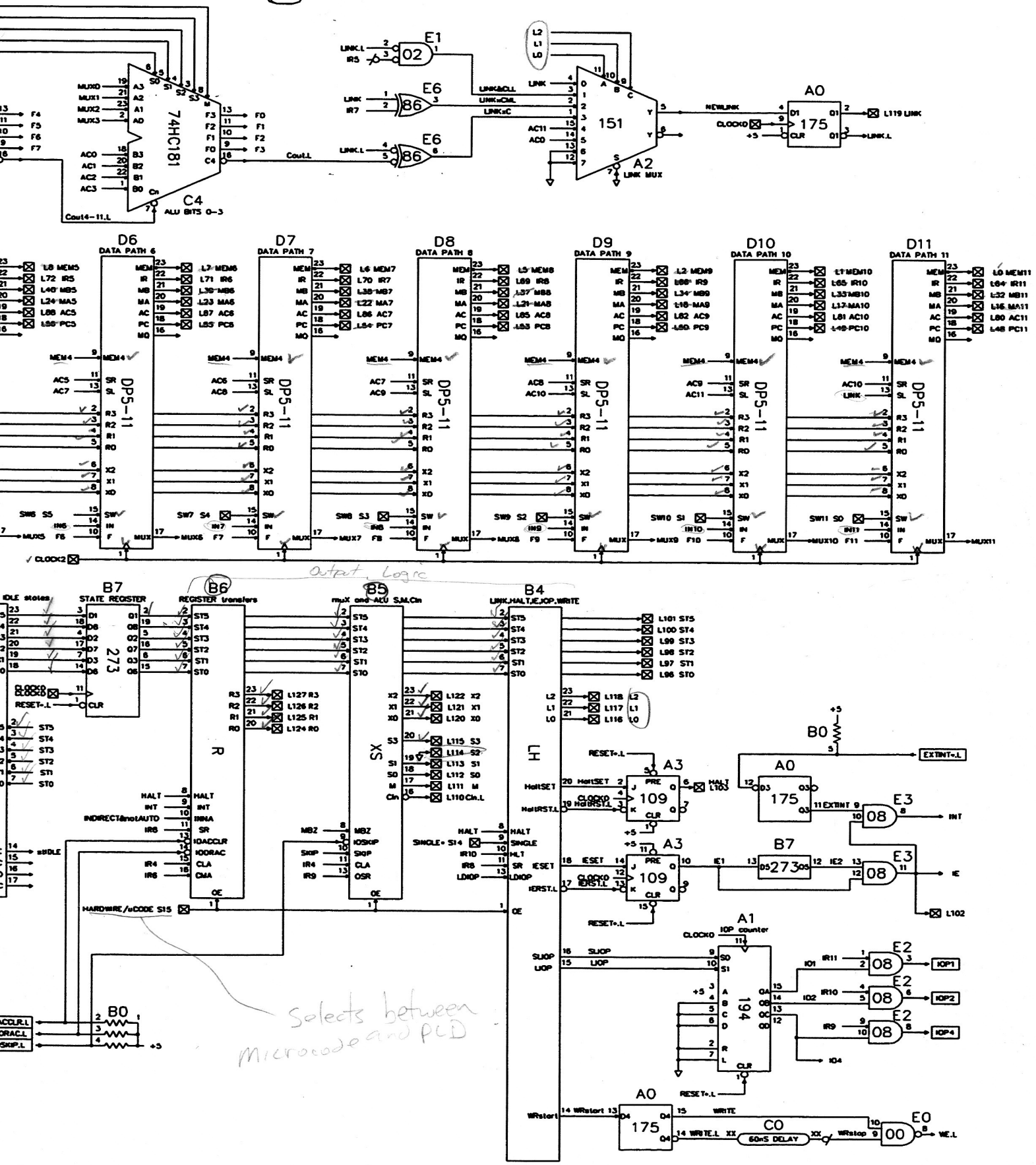

PDP8 Circu
C1
MEMORY BITS 0-3
C2
MEMORY BITS 4-7
C3
MEMORY BITS 8-11
CY7C168
74HC181
C9
ALU BITS 8-11
C6
ALU BITS
D0
DATA PATH 0
D1
DATA PATH 1
D2
DATA PATH 2
D3
DATA PATH 3
D4
DATA PATH 4
D5
DATA PA
DP0-4
DP5-11
CLOCK1
B11
States from IDLE
IDLE
B10
Branch to EXECUTE states
EXEC
B9
GROUP 1 states
G1X
INCREMENT and
E7
IO address ZERO
E8
MA0-7 ZERO
E9
MB0-7 ZERO
E11
MB8-11 ZERO
E10
AC0-7 ZERO
E11
AC8-11 ZERO
E3
E4
E5
E6
E0
E1
A0
B7
4078
4002
08
00
10
32
175
273
86
02
Next State
Enable
Busses?
XS OE
60ns Delay
INs are next Semester

it Diagram

1/14/91

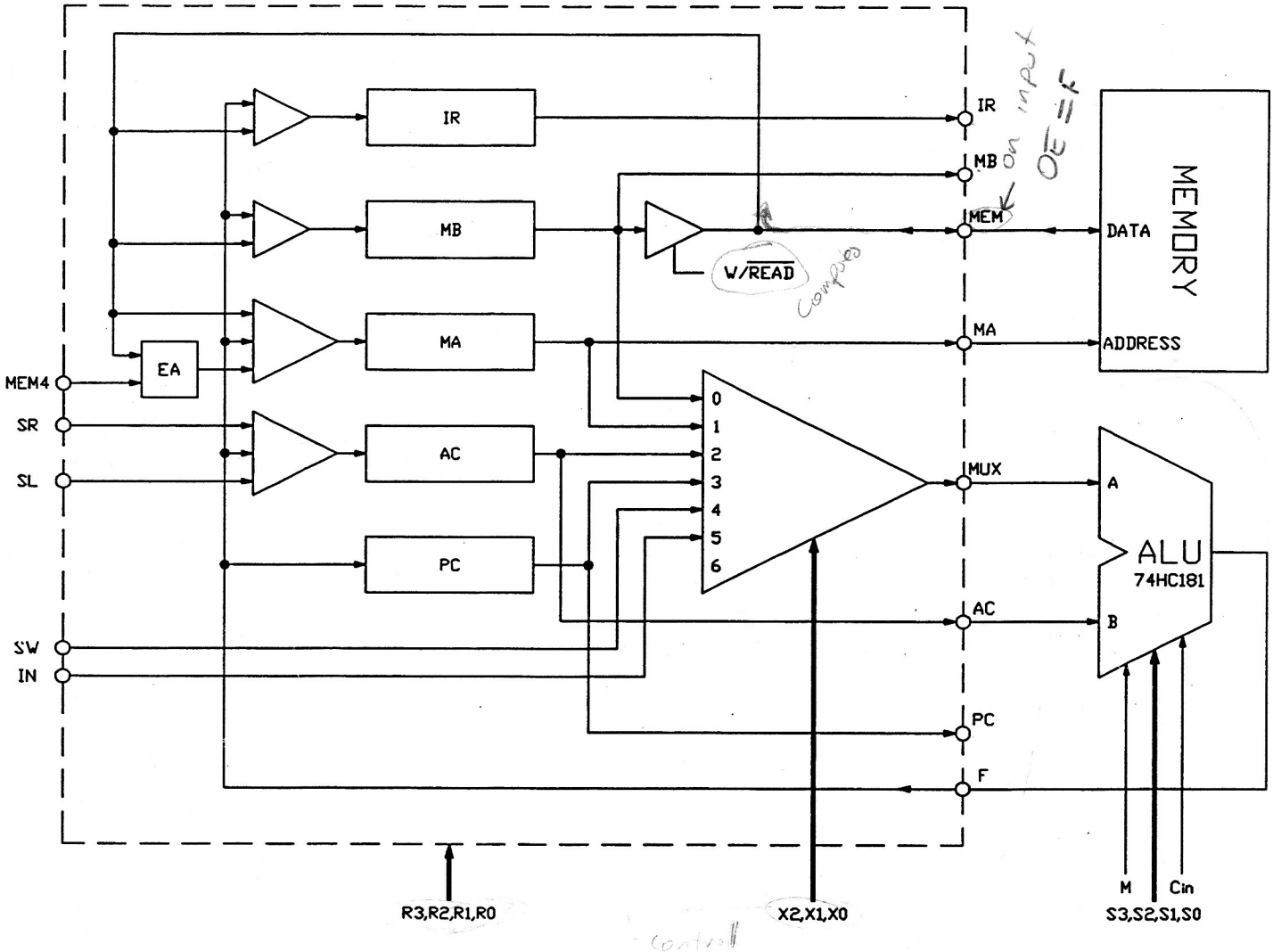


11/5/90

PDP8 DATA PATH

DATA PATH PAL

20G10



REGISTER TRANSFER

R3,R2,R1,R0		MEM	IR	MB	MA	AC	PC	Transfer Description
0000	HOLD							
0001	IR<M		MEM		EA		F	IR<MEM PC<F MA<EA
0010	SR<AC					SR		SR<AC
0011	IR<F		F					IR<F
0100	MB<M			MEM				MB<MEM
0101	MX<M			MEM	MEM			MB<MEM MA<MEM
0110	SL<AC					SL		SL<AC
0111	-							
1000	MB<F			F				MB<F
1001	MA<F				F			MA<F
1010	AC<F					F		AC<F
1011	PC<F						F	PC<F
1100	M<MB	MB						M<MB
1101	MMA<F	MB			F			MA<F M<MB
1110	MAC<F	MB				F		AC<F M<MB
1111	MPC<F	MB					F	PC<F M<MB

Source(s)

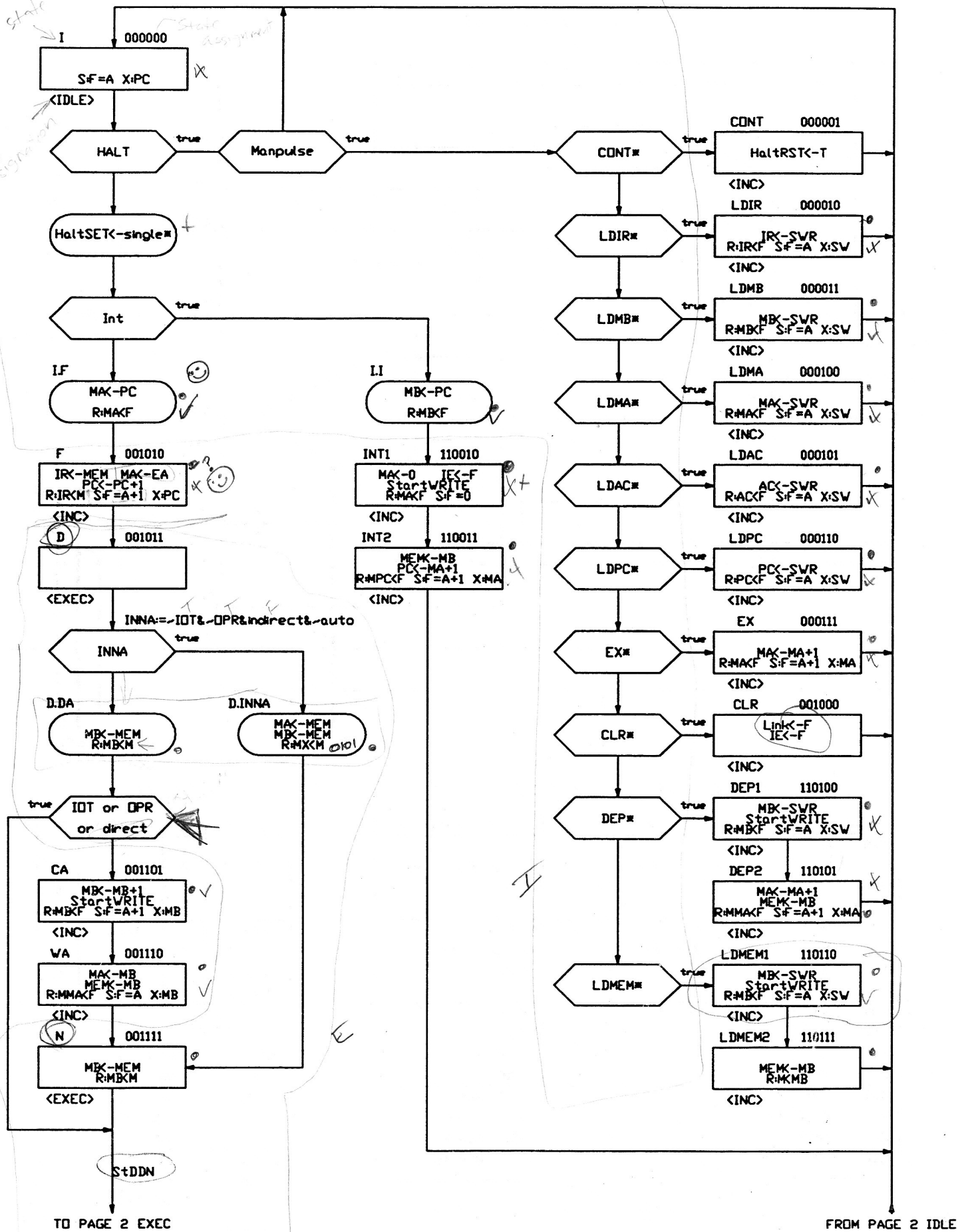
ALU

ALU OP	M	S3,S2,S1,S0	Cin
F=0	1	0011	0
F=A	0	0000	0
F=B	1	1010	0
F=~A	1	0000	0
F=A+1	0	0000	1
F=A+B	0	1001	0
F=A|B	0	0001	0
F=A&B	0	1011	1

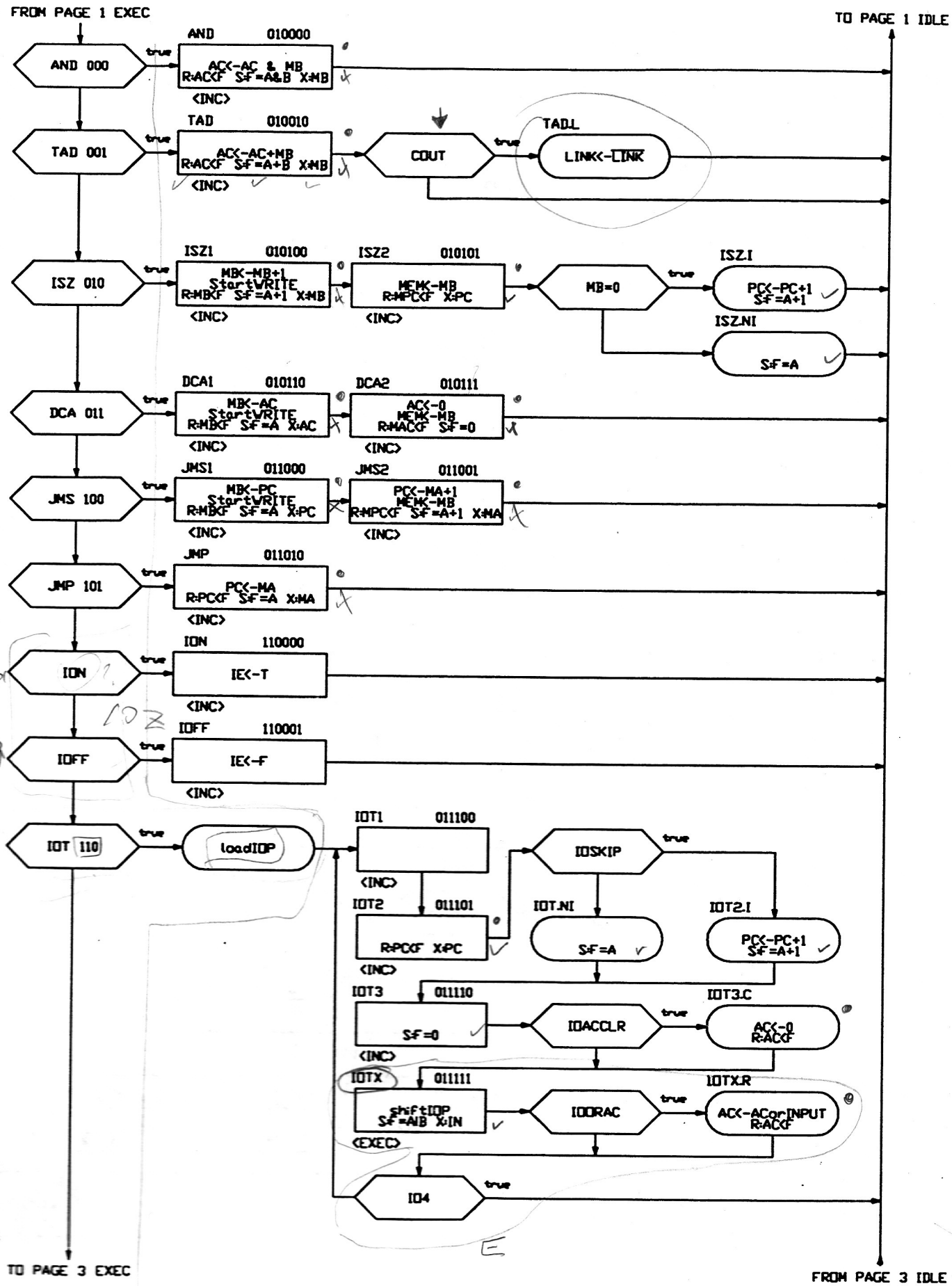
MUX

MUX OUT	X2,X1,X0
MB	000
MA	001
AC	010
PC	011
SW	100
IN	101
-	110
-	111

PDP8 ASM Chart



PDP8 ASM Chart



PDP8 ASM Chart