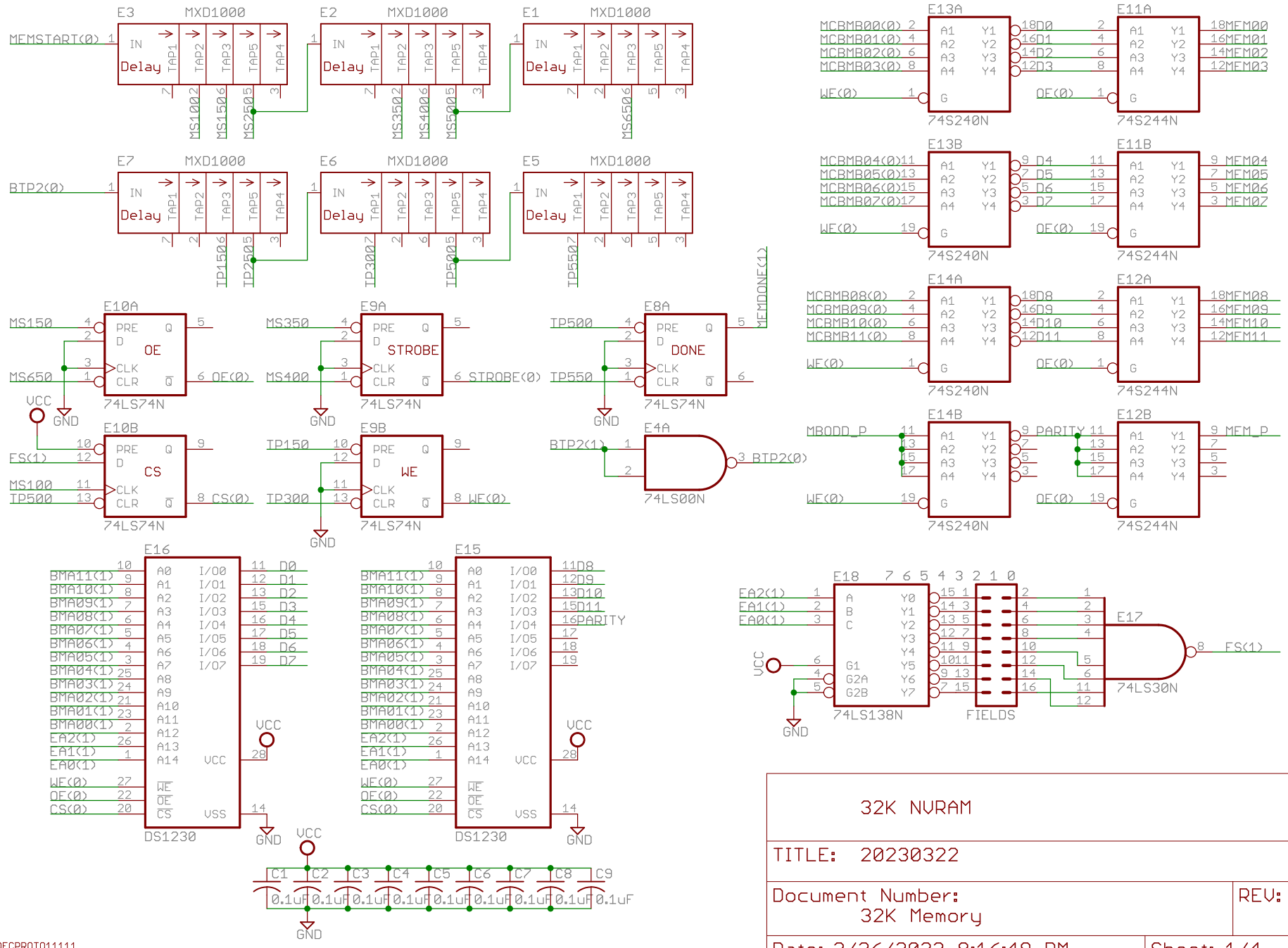

32K NVRAM

TITLE: 20230322

Document Number: 32K Memory

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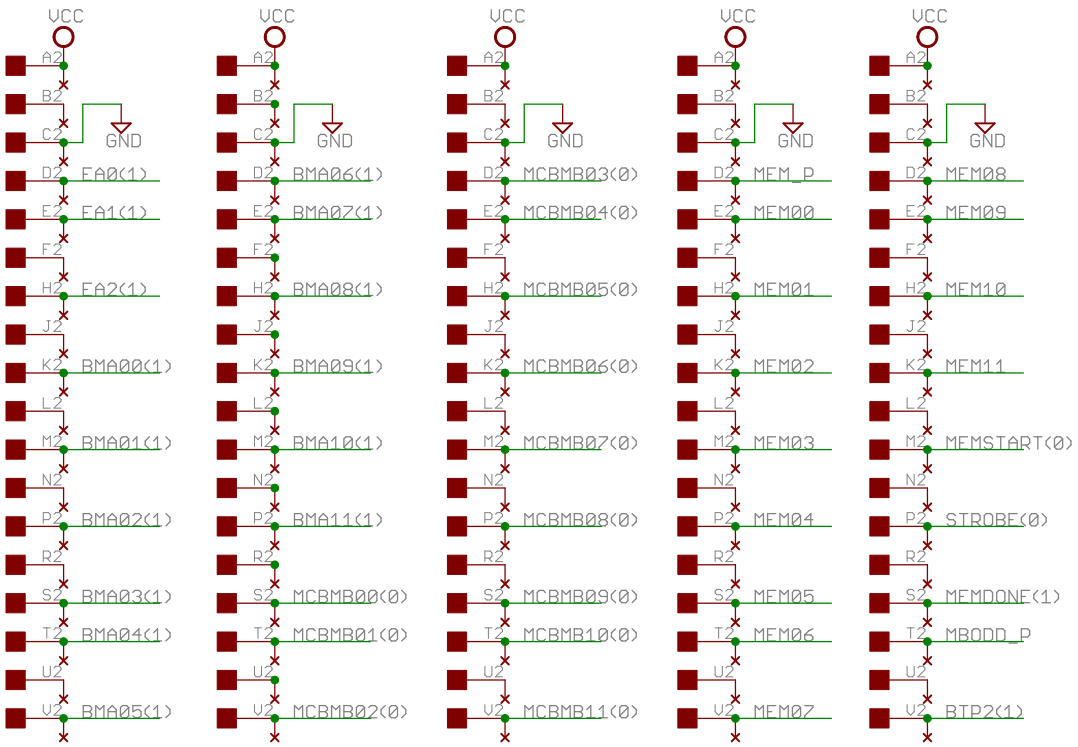
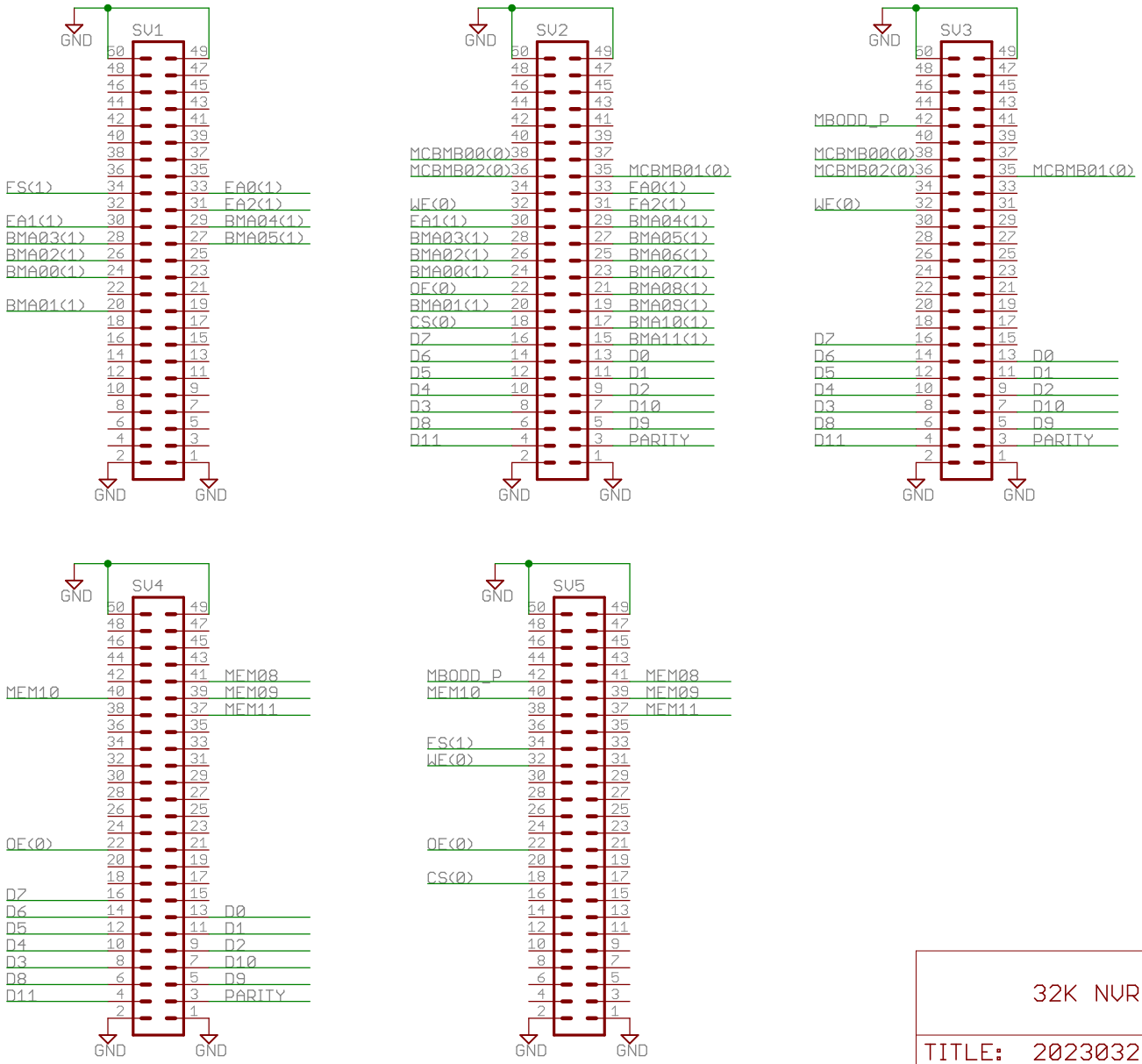


32K NVRAM		
TITLE: 20230322		
Document Number: Computer Connectors		REV:
Date: 3/26/2023 8:16:49 PM	Sheet: 2/4	



32K NVRAM	
TITLE: 20230322	
Document Number: Board Interconnect	REV:
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MM8I Notes:

The CPU initiates a read-modify-write cycle with a MEM_START pulse.

150 ns later MEM_BEGIN sets at the beginning of READ.

150 ns or more later STROBE is sent when the CPU should grab the READ data.

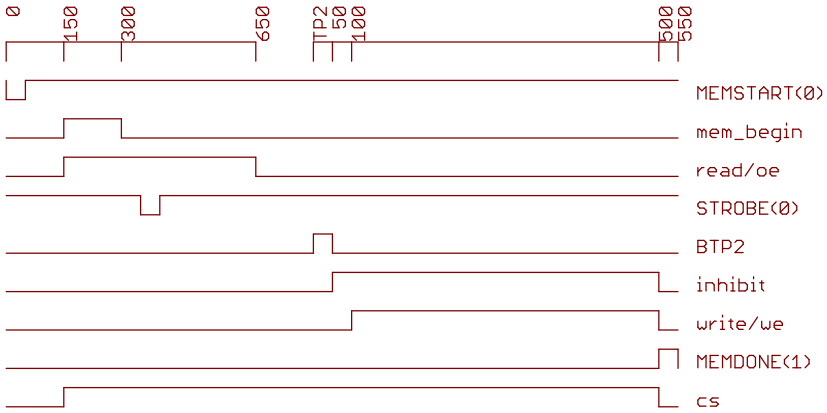
350 ns later, READ ends.

50 ns after TP2, INHIBIT begins.

100 ns after TP2, WRITE is asserted.

400 ns after WRITE begins, WRITE ends and MEM_DONE is sent to the CPU.

Lowercase signifies a local signal, not used by the CPU.



32K NVRAM		
TITLE: 20230322		
Document Number: Notes		REV:
Date: 3/26/2023 8:16:49 PM	Sheet: 4/4	